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A VARIABLE BANDWIDTH FILTER AMPLIFIER

A THESIS

Presented to

The Faculty of the Graduate Division

By

Robert Stewart Eads

In Partial Fulfillment

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Master of Science in Electrical Engineering

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A VARIABLE BANDWIDTH FILTER AMPLIFIER

Approved:

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Date approved by Chairman: June 8, 1964

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SUMMARY

The parallel-T network has been used extensively in the feedback loops of amplifiers to produce highly selective filter amplifiers. However, previously constructed circuits are not able to continuously vary the overall circuit Q-factor while maintaining a constant center frequency and a constant gain at center frequency.

The selective amplifier proposed here uses a parallel-T network in the feedback loop, which produces an overall response like that of a parallel RLC network driven with a constant current. In fact, a special RC load circuit is placed on the amplifier's output so that the equation governing the overall voltage gain will be identical in form to the equation for the parallel RLC network. This arrangement allows variation of the overall Q-factor from a value less than .5 to a value of approximately 500 while maintaining a constant center frequency at 1 kc/s and a constant gain at center frequency. Transistors and RC circuitry are exclusively employed.

A three stage transistor amplifier is used to provide the necessary voltage gain. The input stage is a summing amplifier which adds the input signal to the signal fed back from the parallel-T network. The input stage has a high input resistance to prevent loading down the parallel-T. A common-emitter common-emitter compound connection of transistors is employed to obtain this high input resistance. Also, special consideration is given to the design of the amplifier section in order that oscillations will not result. Additional consideration is given to

achievement of a fairly high signal-to-noise ratio at the output.

A systematic method for calculating the element values in the parallel-T and load circuits is presented along with equations to predict the maximum Q attainable with the voltage gain present. All circuit elements are given in terms of one element and criteria are established for determination of this one element.

The proposed circuit was constructed and measurements were made to check its operation with that predicted. The amplifier section is considered stage by stage to illustrate the manner in which the overall amplifier response is achieved. In addition, the effects of varying the d.c. supply voltage and the ambient temperature are considered to determine the stability of the circuit to such changes. The overall operation of the constructed circuit was satisfactory which indicates that a complete solution of the proposed problem is feasible. However, the circuit constructed did have certain disadvantages; these are outlined along with possible ways to avoid or reduce them.

CHAPTER I

INTRODUCTION

It is possible to achieve high-Q circuits at audio frequencies by the introduction of a rejection-type network, such as the parallel-T, into the feedback loop of an amplifier. Highly selective amplifiers employing parallel-T rejection networks in feedback loops have been widely used at low frequencies in applications where high selectivity, compactness, and low cost are important considerations. Although the parallel-T is commonly employed in amplifier feedback loops to produce a bandpass response a review of the literature has not produced a situation where a specific RC load circuit was used to produce an overall response like the parallel RLC response. To use a parallel RLC circuit at audio frequencies would be difficult because of the physical problems posed by the inductance. Not only are high-Q coils large and expensive, but it would be very difficult to vary inductance continuously in order to change the circuit Q. Also, the literature survey has not produced a case where the effective Q of the overall circuit can be varied continuously by changing the gain in the feedback loop without changing the resonant frequency, f_o, or the gain at the resonant frequency.

The objective of the proposed research is to construct and analyze an active RC circuit which will produce a frequency response similar to that for a parallel RLC network. The proposed circuit will use a parallel-T network in a feedback path and the output will be taken from an RC load circuit. A simplified block diagram representing the proposed research is

shown in Figure 1. The effective Q of the overall circuit can be varied by changing the gain in the feedback loop. As this gain in the feedback loop is changed the gain E_2/E_1 at the resonant frequency, f_o, will not vary. Also, the value of the frequency at maximum gain will not vary. With reference to Figure 1, a frequency response like that for a parallel RLC network can be obtained if the following are true:

(a) Driving point impedance, Z_{11T}, for the feedback network proportional to the driving point impedance, Z_{11L}, for the load circuit

(b) Q_{oT} for the feedback network equal to Q_{oL} for the load circuit

(c) Resonant frequency, ω_{oT}, of the feedback network equal to the resonant frequency, ω_{oL}, for the load circuit

(d) Certain ratios for the circuit elements

In particular,

$$\frac{E_2}{E_1} = \frac{K_e \omega_o}{Q_o(1 + \beta K_o)} \frac{S}{\left(S^2 + S \frac{\omega_o}{Q_o(1+\beta K_o)} + \omega_o{}^2\right)}$$

can be obtained where K_e, ω_o, Q_o and K_o are constants depending on the circuitry. By varying β the effective Q of the entire circuit can be varied. Changing the effective Q will change the bandwidth of the passband according to the equation

$$\text{Bandwidth} = f_o/Q$$

This effect is illustrated in Figure 2. β may be changed by varying a resistor value on the output of the parallel-T.

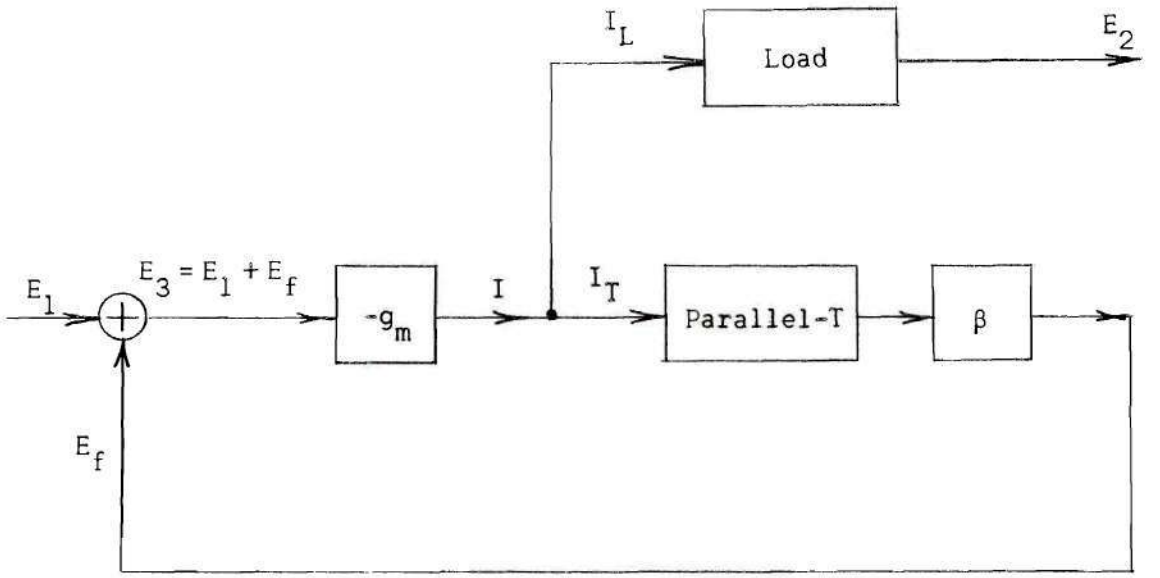


Figure 1. Block Diagram for Proposed Research

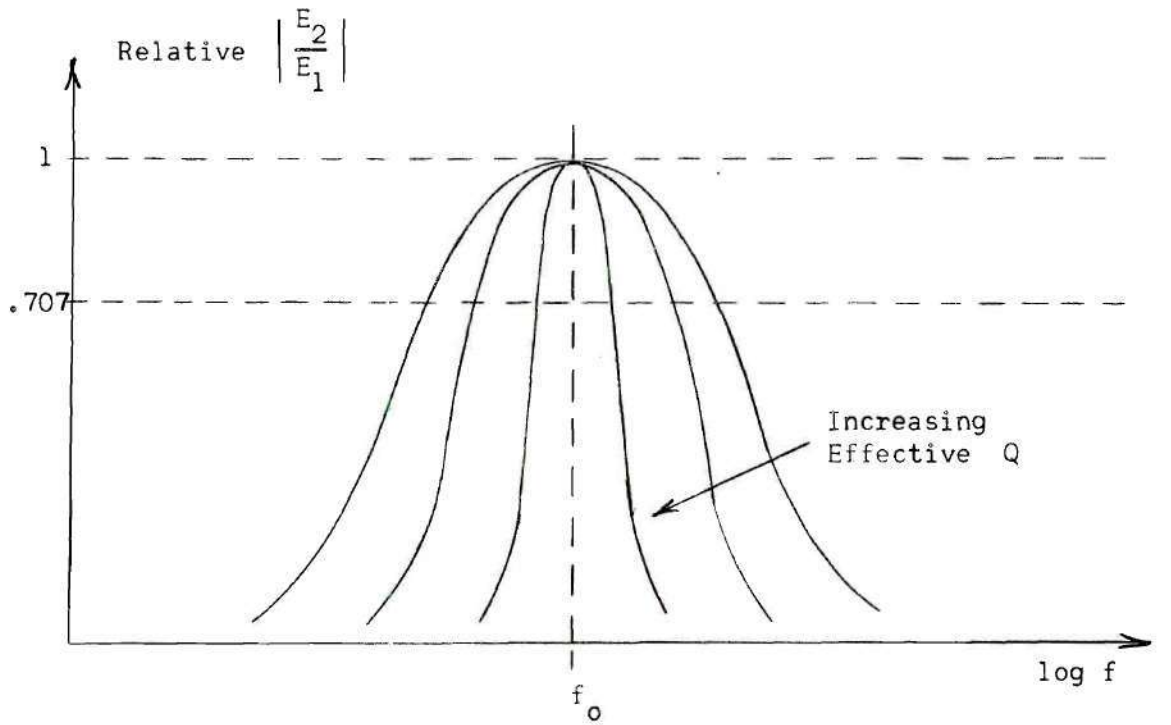


Figure 2. Overall Response for Proposed Circuit.

Figure 3 is a simplified block diagram which represents the basic circuit used in most previous research. Note that the output is taken from the input terminals of the parallel-T, and that no provision has been made for continuously varying the feedback voltage.

Most of the circuits encountered in the literature are designed to obtain one fixed Q, and to change this Q would require a partial redesign. Two such circuits, proposed by A. E. Bachmann (1), are illustrated in Figure 4. Figure 4a shows a very simple circuit with all elements fixed. Since this circuit contains only one transistor stage it should be free from oscillation. However, this and similar circuits have the following disadvantages:

(a) Since the input impedance of the amplifier should not load the parallel-T network appreciably, the source resistance R_g must be large.

(b) In order to get most of the signal available from the amplifier into the parallel-T for high feedback, the load resistance R_L should not be too small.

Because of these two disadvantages Bachmann proposed another circuit as shown in Figure 4b. This circuit uses two common-emitter stages as amplifiers, and the parallel-T network is terminated by a common-collector stage. The load on this stage is essentially the input impedance of the first transistor, T_1, in common base connection and is consequently very low. In order to increase the input impedance of the third stage, the resistance R_{E_3} has been added to the load. Note, however, that both circuits take the output from the input terminals of the parallel-T. Also, neither circuit has provisions for varying the overall Q-factor continuously. Figure

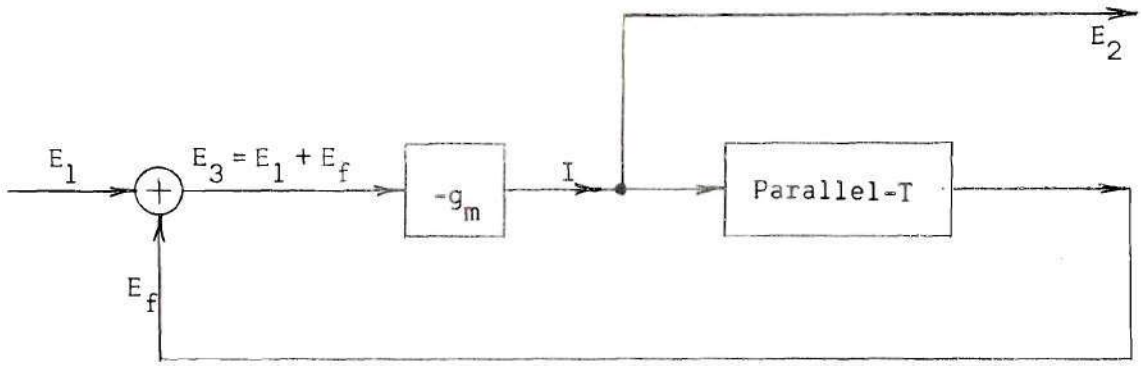


Figure 3. Block Diagram Representing Previous Research.

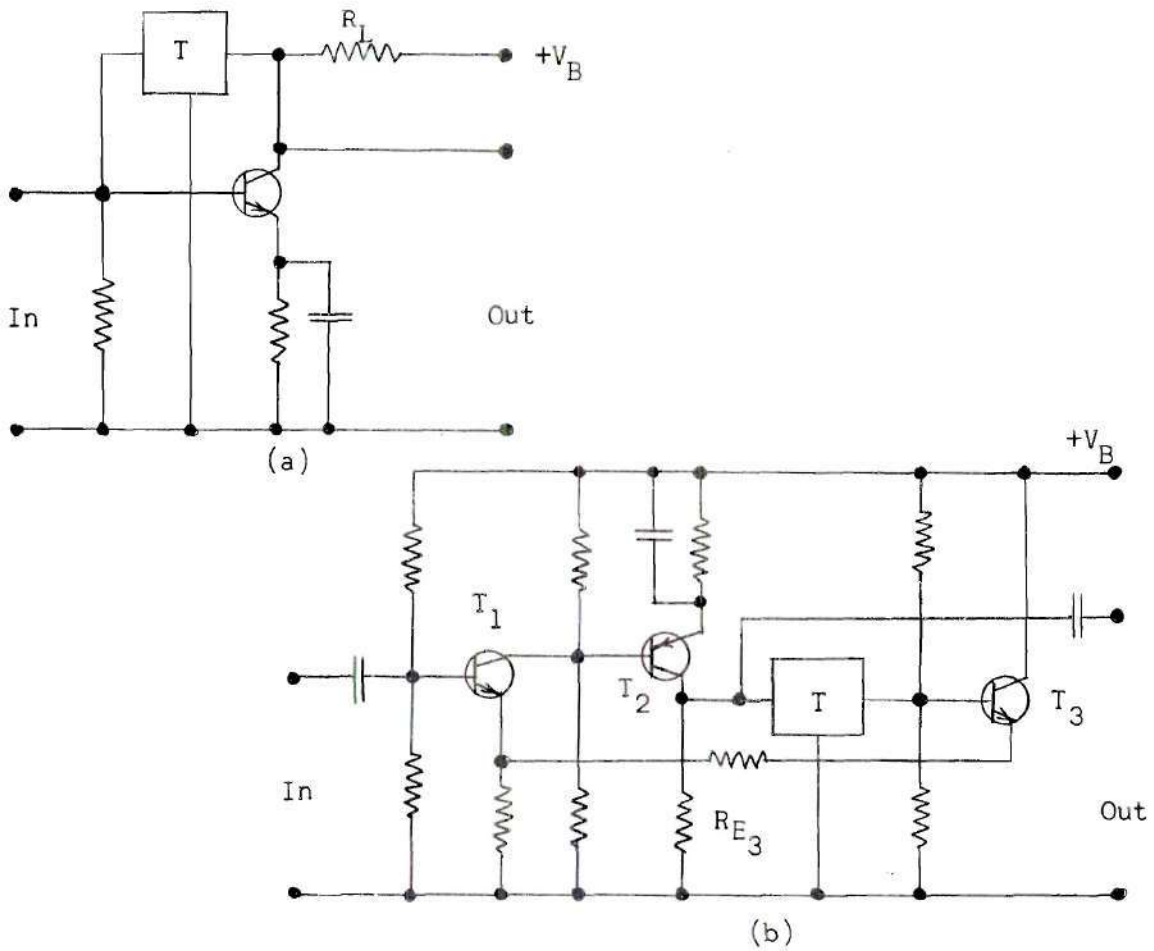
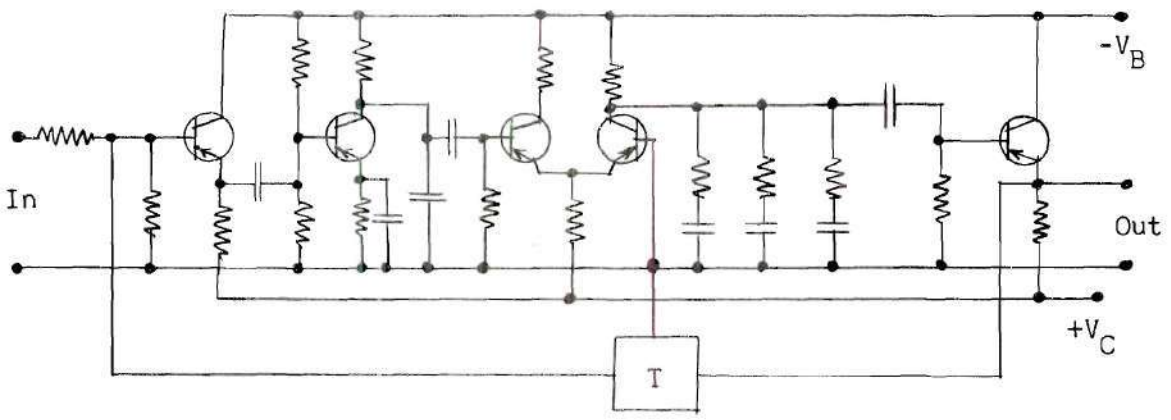


Figure 4. Transistor Active Filters Using Parallel-T Rejection Networks Proposed by A. E. Bachmann.

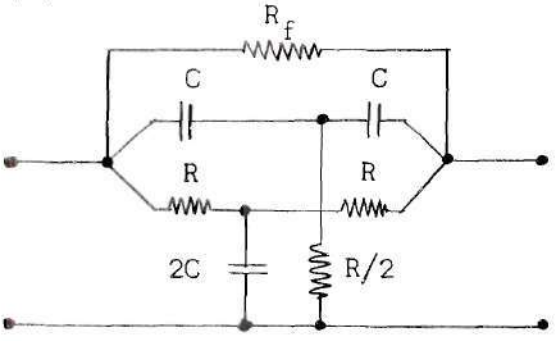
5a illustrates a scheme proposed by R. J. Lamden (2). It is desired that this amplifier have a number of stages each with the same half-power frequency f_c. The amplifier will then have an overall response flat almost to f_c, and then falling rapidly. It is further desired to modify the response of the amplifier by the insertion of networks to give a gain reduction of 33-1/3 db per decade. Figure 5b shows the parallel-T network used by Lamden with a damping resistor R_f across it. By analogy with the tuned parallel LC circuit it seems possible to damp the parallel-T network by putting a resistor R_f in parallel with it. Figure 5c illustrates the overall gain in db plotted against normalized frequency. For this figure $\beta = \frac{2R}{R_f}$ where R and R_f are shown in Figure 5b. For this circuit, control of the overall bandwidth is obtained by changing the value of R_f. Note that the center frequency shifts slightly as R_f and β are varied. Also, note that the gain at center frequency changes slightly as β is varied.

The circuits presented here from articles by Bachmann and Lamden (1, 2) are fairly representative of the literature regarding active filter amplifiers using a rejection network in a feedback loop. The circuit presently proposed in Figure 1 is unique in that Q may be varied continuously while center frequency, and the gain at center frequency, remain constant.

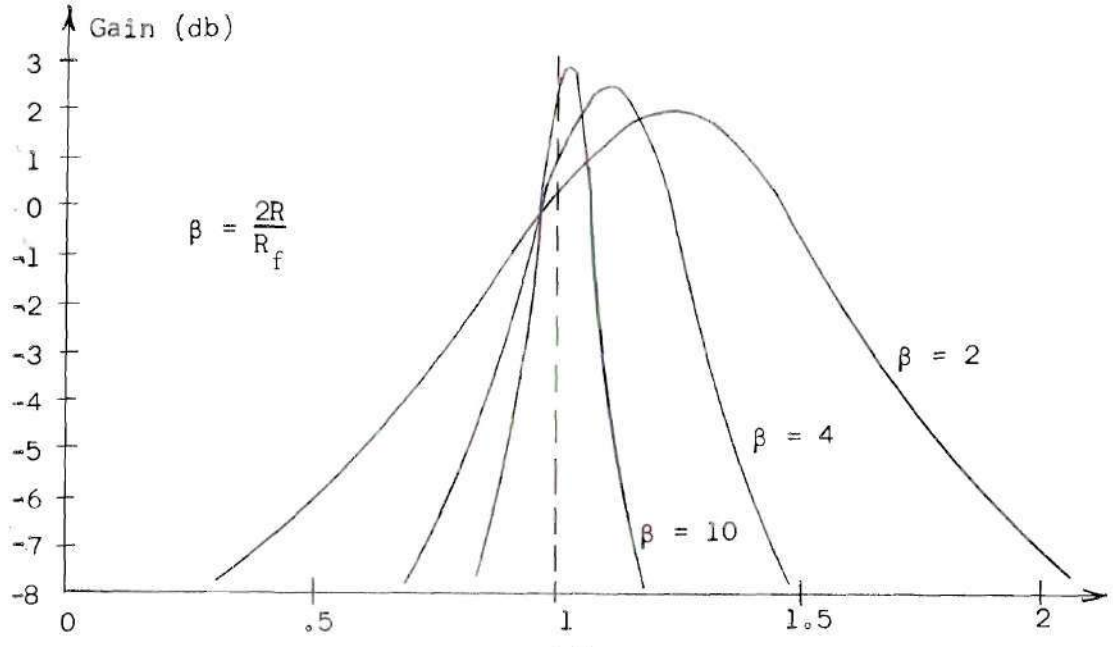
A circuit similar to the one proposed was designed and constructed by Dr. B. J. Dasher using vacuum tubes. The proposed research will employ transistors instead of vacuum tubes.



(a)



(b)



(c)

Figure 5. Transistor Active Filters Proposed by R. J. Lamden Using a Parallel-T Network.

CHAPTER II

BASIC PRINCIPLES

Parallel RLC Network

When the parallel RLC network is driven with a constant current the frequency response will be bandpass.

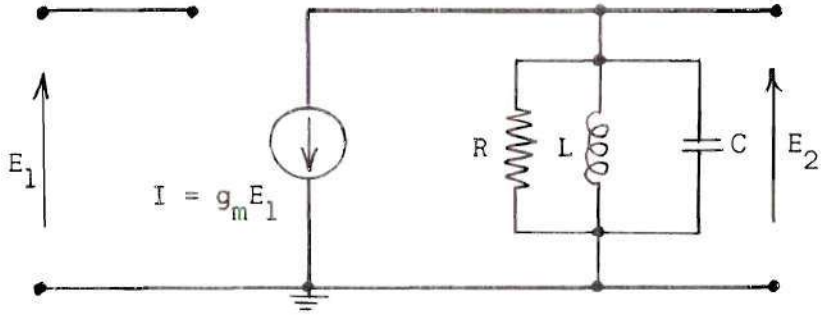


Figure 6. Parallel RLC Network Driven with Voltage Controlled Current Source.

With reference to Figure 6,

$$I = g_m E_1$$

$$E_2 = -IZ = - g_m E_1 Z$$

where Z = impedance of parallel RLC network

$$\frac{E_2}{E_1} = - g_m Z$$

$$Z = \frac{1}{\frac{1}{R} + \frac{1}{SL} + SC} = \frac{1}{C} \left(\frac{S}{S^2 + \frac{S}{RC} + \frac{1}{LC}} \right)$$

For the parallel RLC network the resonant frequency is $\omega_o = \frac{1}{\sqrt{LC}}$, and the circuit Q is $Q_o = R\sqrt{C/L}$. Also,

$$\frac{\omega_o}{Q_o} = \frac{1}{RC}$$

Therefore,

$$\frac{E_2}{E_1} = -\frac{g_m}{C}\left(\frac{S}{S^2 + S\frac{\omega_o}{Q_o} + \omega_o^2}\right)$$

It will be useful to write $1/C$ as

$$\frac{1}{C} = \frac{Q_o/C}{Q_o} = \frac{RC\omega_o/C}{Q_o} = \frac{R\omega_o}{Q_o}$$

and

$$\frac{E_2}{E_1} = -\frac{g_m R\omega_o}{Q_o}\left(\frac{S}{S^2 + S\frac{\omega_o}{Q_o} + \omega_o^2}\right)$$

Now let $-g_m R = K_e$ = gain at ω_o. So,

$$\frac{E_2}{E_1} = \frac{K_e\omega_o}{Q_o}\left(\frac{S}{S^2 + S\frac{\omega_o}{Q_o} + \omega_o^2}\right) \qquad (1)$$

$$= \frac{K_e}{Q_o}\left(\frac{j\omega\omega_o}{(\omega_o^2 - \omega^2) + j\omega\frac{\omega_o}{Q_o}}\right)$$

$$= \frac{K_e}{Q_o}\left(\frac{j\rho}{(1 - \rho^2) + j\frac{\rho}{Q_o}}\right)$$

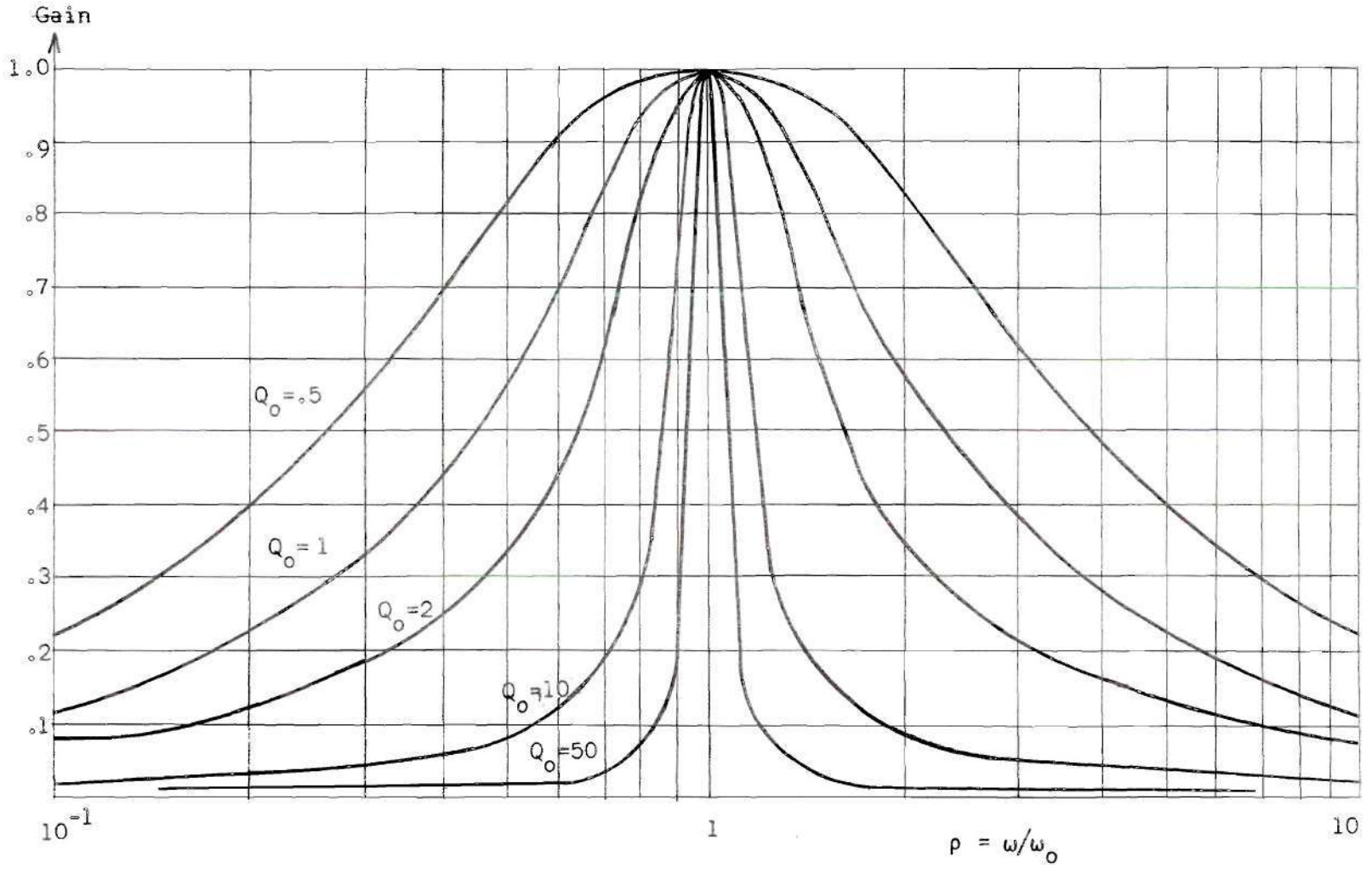


Figure 7. Normalized Parallel RLC Network Response for Various Values of Q_o.

where $\rho = \omega/\omega_o$

$$\left|\frac{E_2}{E_1}\right| = \frac{K_e \rho}{Q_o} \frac{1}{\sqrt{(1-\rho^2)^2 + (\frac{\rho}{Q_o})^2}}$$

This is plotted in Figure 7 for $K_e = 1$ and for several values of Q_o. It will now be shown that the half-power bandwidth is f_o/Q_o for this response.

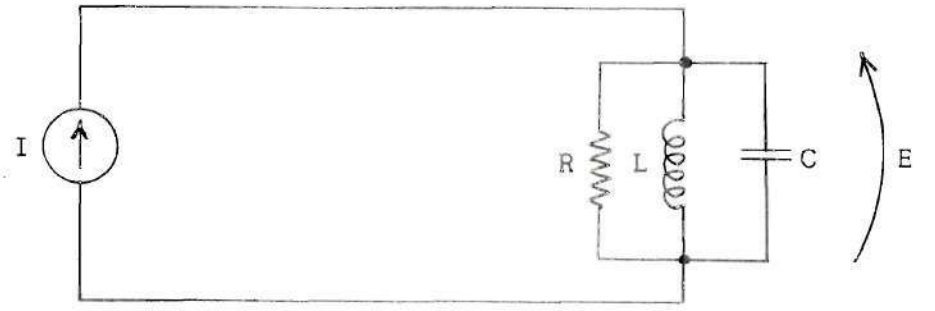


Figure 8. Parallel RLC Network Driven with Constant Current.

With reference to Figure 8,

$$I = E(\frac{1}{R} + \frac{1}{SL} + SC)$$

or rewriting,

$$\frac{E}{I} = \frac{j\omega RL}{R(1 - \omega^2 LC) + j\omega L}$$

At resonance $\omega_o = \frac{1}{\sqrt{LC}}$, and $E_{\omega_o} = IR$. At the half-power points, ω_3,

$$E_{\omega_3} = \frac{E_{\omega_o}}{\sqrt{2}} = \frac{IR}{\sqrt{2}}$$

$$\left|\frac{E}{I}\right|_{\omega_3} = \frac{R}{\sqrt{2}} = \frac{\omega_3 RL}{\sqrt{R^2(1-\omega_3^2 LC)^2 + \omega_3^2 L^2}}$$

Squaring both sides,

$$\frac{1}{2} = \frac{\omega_3^2 L^2}{R^2(1-\omega_3^2 LC)^2 + \omega_3^2 L^2}$$

Using $R = Q_o \omega_o L$ and $\omega_o^2 = \frac{1}{LC}$, the last relation can be written as

$$Q_o^2 \omega_o^2 - 2Q_o \omega_3^2 + Q_o^2 \frac{\omega_3^4}{\omega_o^2} - \omega_3^2 = 0$$

or,

$$\omega_3^4 \left(\frac{Q_o^2}{\omega_o^2}\right) - \omega_3^2 (1 + 2Q_o^2) + Q_o^2 \omega_o^2 = 0$$

Solving for ω_3 and omitting negative frequencies,

$$\omega_3 = \sqrt{\frac{(1 + 2Q_o^2) \pm \sqrt{1 + 4Q_o^2}}{2Q_o^2/\omega_o^2}}$$

Half-power bandwidth = $f_h - f_l = \frac{\omega_{3h} - \omega_{3l}}{2\pi}$ where

$$\omega_{3h} = \sqrt{\frac{(1 + 2Q_o^2) + \sqrt{1 + 4Q_o^2}}{2Q_o^2/\omega_o^2}}$$

and

$$\omega_{3l} = \sqrt{\frac{(1 + 2Q_o^2) - \sqrt{1 + 4Q_o^2}}{2Q_o^2/\omega_o^2}}$$

From the above it can be shown that

$$(\text{Bandwidth})^2 = \frac{\omega_o^2}{(2\pi)^2 Q_o^2} = \frac{f_o^2}{Q_o^2}$$

or that

$$\text{Bandwidth} = \frac{f_o}{Q_o} \qquad (2)$$

With careful design and the use of magnetic ferrite cores, circuits using inductors may produce Q's on the order of several hundred at high audio frequencies, but the increase in the bulk and cost of the coils makes them less suitable as frequency is reduced. Also, suppose it is desired to continuously vary the circuit Q while maintaining a constant center frequency and a constant gain at center frequency. This would be very difficult to achieve using the parallel RLC circuit as can be seen from Equation (1). For the gain at center frequency, $K_e = -g_m R$, to remain constant R must remain constant. To continuously vary the circuit Q, $Q = R\sqrt{\frac{C}{L}}$, L and C must be varied simultaneously while keeping $\omega_o = \frac{1}{\sqrt{LC}}$ constant. This is indeed a difficult task.

By introducing a rejection-type network, such as the bridged-T or the parallel-T, into the feedback loop of an amplifier bandpass characteristics similar to those of single tuned circuits can be obtained.

Proposed Circuit

The proposed circuit will use a parallel-T rejection network in the feedback loop of an amplifier and will use a special load circuit to give an overall response like that of the parallel RLC network.

At this point it will be sufficient to simply state the desired transfer impedances for both the parallel-T and load circuits. They are

now stated exactly as they will later be derived:

$$Z_{21T} = \frac{1}{2}\left(\frac{1}{G_o + G_a + G_b}\right)\left(\frac{S^2 + \omega_o^2}{S^2 + S\frac{\omega_o}{Q_o} + \omega_o^2}\right) \tag{3}$$

where G_o, G_a and G_b are circuit elements, Q_o is the parallel-T Q-factor, and ω_o is the resonant frequency at which the notch occurs.

$$Z_{21L} = \frac{G_2}{C_2(G_1 + G_2)}\left(\frac{S}{S^2 + S\frac{\omega_o}{Q_o} + \omega_o^2}\right) \tag{4}$$

where G_1, G_2 and C_2 are circuit elements, Q_o is the load circuit Q-factor, and ω_o is the resonant frequency.

A subscript "T" will indicate the parallel-T, and a subscript "L" will indicate the load circuit. For the present the following will be accepted:

$$\omega_{oT} = \omega_{oL} = \omega_o$$

$$Q_{oT} = Q_{oL} = Q_o$$

These relations will later be made true.

With reference to Figure 9, β is an attenuator and may be part of the parallel-T network (i.e. a potentiometer that is also the load resistance for the parallel-T). The loading effect will be included in the transfer function Z_{21T}, but the voltage ratio is specified separately as β.

It will be necessary to have the driving point impedances, Z_{11T} and Z_{11L}, proportional at all frequencies:

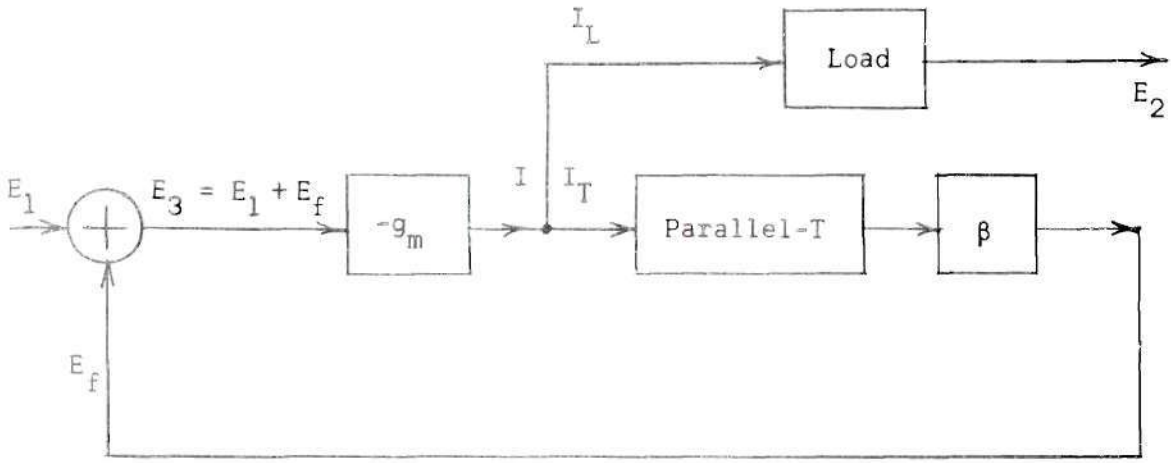


Figure 9. Simplified Block Diagram of Proposed Circuit.

Z_{11T} proportional to Z_{11L} or

$$Z_{11T} = KZ_{11L} \tag{5}$$

So

$$I_T = I\left(\frac{Z_{11L}}{Z_{11T} + Z_{11L}}\right) = I\left(\frac{Z_{11L}}{KZ_{11L} + Z_{11L}}\right) = I\left(\frac{1}{K+1}\right)$$

and similarly,

$$I_L = I\left(\frac{K}{K+1}\right)$$

Let $I_T = Ik$ (i.e. $k = \frac{1}{K+1}$). So

$$K = \frac{1-k}{k}$$

$$I_L = I\left(\frac{K}{K+1}\right) = I(1-k)$$

$$I = -g_m E_3$$

$$E_3 = E_1 + E_f = E_1 + I_T Z_{21T} \beta = E_1 + IkZ_{21T} \beta$$

$$= E_1 - g_m E_3 k Z_{21T} \beta$$

Solving for E_3,

$$E_3 = \frac{E_1}{1 + g_m k \beta Z_{21T}} \tag{6}$$

$$E_2 = I_L Z_{21L} = I(1 - k) Z_{21L} = - g_m E_3 (1 - k) Z_{21L}$$

Now substitute E_3 as given in Equation (6).

$$E_2 = \frac{- g_m E_1 (1 - k) Z_{21L}}{1 + g_m k \beta Z_{21T}}$$

and,

$$\frac{E_2}{E_1} = \frac{-g_m (1 - k) Z_{21L}}{1 + g_m k \beta Z_{21T}}$$

Using Equations (3) and (4) for Z_{21T} and Z_{21L} respectively there results

$$\frac{E_2}{E_1} = \frac{-g_m (1 - k) \frac{G_2}{C_2 (G_1 + G_2)} \left(\frac{S}{S^2 + S \frac{\omega_o}{Q_o} + \omega_o^2} \right)}{1 + \frac{g_m k \beta}{2} \left(\frac{1}{G_o + G_a + G_b} \right) \left(\frac{S^2 + \omega_o^2}{S^2 + S \frac{\omega_o}{Q_o} + \omega_o^2} \right)}$$

Let

$$\frac{g_m k \beta}{2} \left(\frac{1}{G_o + G_a + G_b} \right) = K_o \beta \qquad (7)$$

It should be noted that $K_o\beta$ equals the open loop gain of the feedback loop as $\omega \rightarrow \infty$.

When $S^2 = -\omega_o^2$,

$$\frac{E_2}{E_1} = -g_m(1 - k) \frac{G_2}{C_2(G_1 + G_2)} \left(\frac{S}{S \frac{\omega_o}{Q_o}} \right)$$

$$= - g_m(1 - k) \frac{G_2}{C_2(G_1 + G_2)} \left(\frac{Q_o}{\omega_o} \right) = K_e$$

where K_e is the constant gain at resonance. Thus it can be written that

$$\frac{E_2}{E_1} = \frac{\frac{K_e \omega_o}{Q_o} S / (S^2 + S \frac{\omega_o}{Q_o} + \omega_o^2)}{1 + \beta K_o (S^2 + \omega_o^2) / (S^2 + S \frac{\omega_o}{Q_o} + \omega_o^2)}$$

which reduces to

$$\frac{E_2}{E_1} = \frac{K_e \omega_o}{Q_o (1 + \beta K_o)} \frac{S}{(S^2 + S \frac{\omega_o}{Q_o (1 + \beta K_o)} + \omega_o^2)} \qquad (8)$$

This response is equivalent to that of the parallel RLC circuit. (Compare Equation (1) for the parallel RLC circuit with Equation (8) for the proposed

circuit). The gain at resonance is independent of βK_o, but the effective Q is proportional to $(1 + \beta K_o)$. That is,

$$\text{Effective } Q = Q_o(1 + \beta K_o)$$

By varying β the bandwidth of the response is varied, but the gain at resonance is fixed at K_e. That is,

$$\text{Bandwidth of response} = \frac{f_o}{Q_o(1 + \beta K_o)}$$

Here, Equation (2), which was derived for the parallel RLC circuit, has been used. This is, of course, permissible because of the equivalence between the two responses. If the load circuit is omitted and the output taken at the input to the parallel-T the numerator of $\frac{E_2}{E_1}$ will be a quadratic. For high Q's the response near resonance will not be very different, but for low Q's the difference is substantial.

Parallel-T Feedback Network

The transfer and driving point impedances for the parallel-T will now be derived. The transfer impedance will be considered first, and it will be derived to correspond with Equation (3).

Figure 10 illustrates the parallel-T as it is to be used in the following analysis. Note the admittance G_o on the input and output of the parallel-T in Figure 10a. G_o on the output will be the β network (i.e. a potentiometer) in Figure 9. G_o is also placed on the input terminals to preserve symmetry. This symmetry is presented clearly in Figure 10b. Now consider a half section of the symmetrical network. Figure 10c shows this half section with its output terminals open, and Figure 10d shows its output

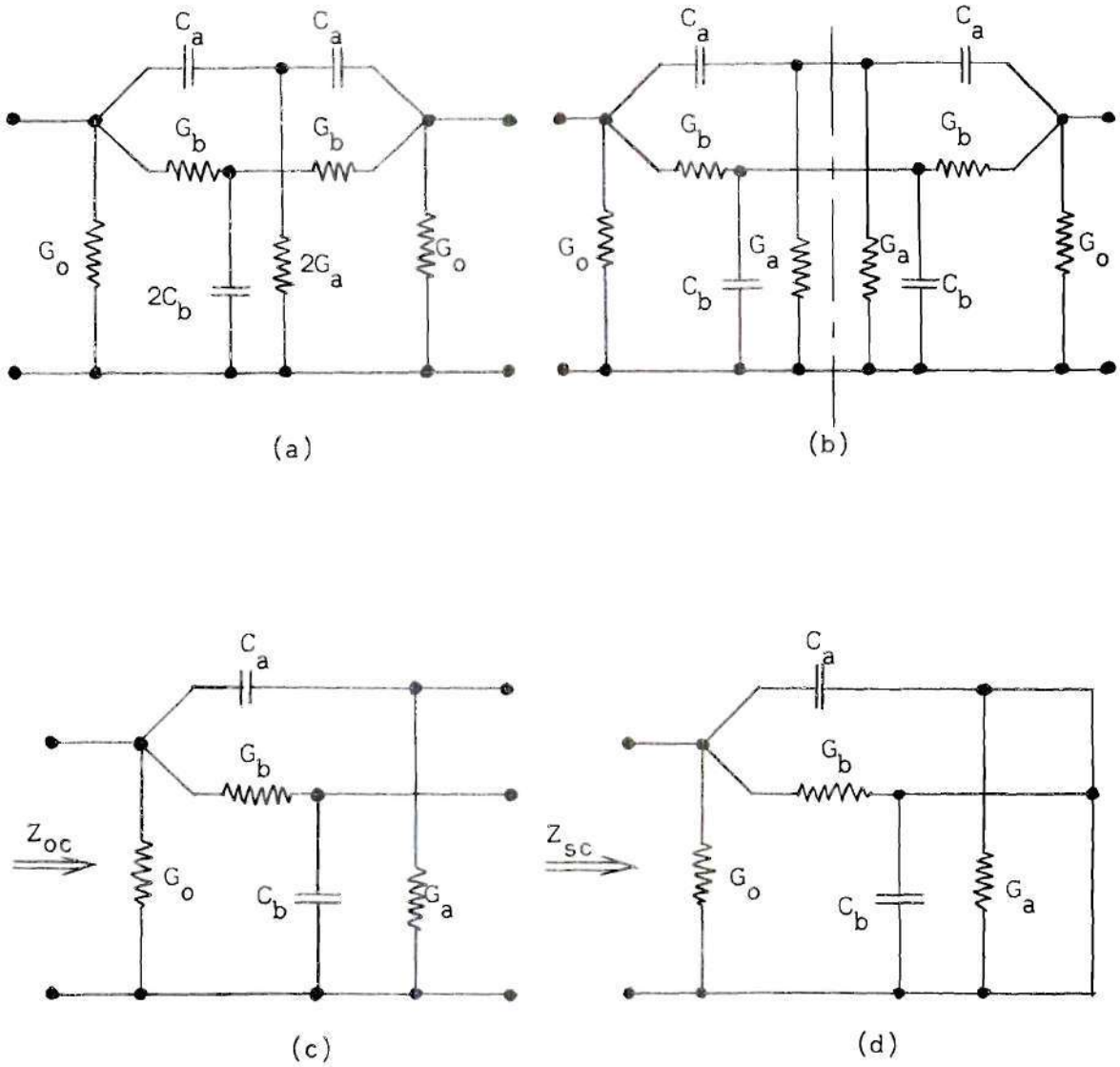


Figure 10. Parallel-T Feedback Network.

terminals shorted together. By Bartlett's bisection theorem the following is true:

$$Z_{oc} \text{ in Figure 10c} = Z_{11T} + Z_{21T}$$

$$Z_{sc} \text{ in Figure 10d} = Z_{11T} - Z_{21T}$$

where Z_{21} = transfer impedance for parallel-T and

Z_{11} = driving point impedance for parallel-T.

From this it follows that

$$Z_{11T} = \frac{1}{2}(Z_{oc} + Z_{sc})$$

$$Z_{21T} = \frac{1}{2}(Z_{oc} - Z_{sc})$$

From inspection of Figure 10c it can be written that

$$Z_{oc} = \frac{1}{G_o + \dfrac{G_b SC_b}{G_b + SC_b} + \dfrac{G_a SC_a}{G_a + SC_a}} \tag{9}$$

and from Figure 10d

$$Z_{sc} = \frac{1}{G_o + G_b + SC_a} \tag{10}$$

Now $Z_{21T} = \frac{1}{2}(Z_{oc} - Z_{sc})$

$$= \frac{1}{2}\left(\frac{1}{G_o + \dfrac{G_b SC_b}{G_b + SC_b} + \dfrac{G_a SC_a}{G_a + SC_a}} - \frac{1}{G_o + G_b + SC_a}\right)$$

which can be rewritten as

$$Z_{21T} = \frac{1}{2}\left(\frac{S^3(C_a^2C_b) + S^2(G_bC_a^2) + S(G_b^2C_a) + G_aG_b^2}{S^3(\nu) + S^2(\eta) + S(\mu) + (\gamma)}\right) \qquad (11)$$

where

$$\nu = G_oC_a^2C_b + G_bC_a^2C_b + G_aC_a^2C_b$$

$$\eta = 2G_oG_bC_aC_b + 2G_aG_bC_aC_b + 2G_aG_oC_aC_b + G_b^2C_aC_b + G_o^2C_aC_b + G_oG_bC_a^2 + G_aG_bC_a^2$$

$$\mu = G_o^2G_bC_a + G_o^2G_aC_b + G_b^2G_oC_a + G_b^2G_aC_b + G_b^2G_aC_a + 2G_oG_aG_bC_b + 2G_oG_aG_bC_a$$

$$\gamma = G_o^2G_aG_b + G_oG_aG_b^2$$

It should be recalled that the desired form for Z_{21T} is

$$\frac{S^2 + \omega_o^2}{S^2 + S\frac{\omega_o}{Q_o} + \omega_o^2}.$$

First, put the numerator of Equation (11) in form of $(S^2 + \omega_o^2)$.

$$\text{Numerator} = S^3(C_a^2C_b) + S^2(G_bC_a^2) + S(G_b^2C_a) + G_aG_b^2$$

$$= C_a^2C_b[S^3 + S^2(G_b/C_b) + S(G_b^2/C_aC_b) + G_aG_b^2/C_a^2C_b]$$

$$= C_a^2C_b[S^3 + S^2a + S\omega_o^2 + a\omega_o^2]$$

$$= C_a^2C_b[(S^2 + \omega_o^2)(S + a)]$$

where $a = G_b/C_b$, $\omega_o^2 = G_b^2/C_aC_b$, and $a\omega_o^2 = G_aG_b^2/C_a^2C_b$.

This requires $\left(\frac{G_b}{C_b}\right)\left(\frac{G_b^2}{C_a C_b}\right) = \frac{G_a G_b^2}{C_a^2 C_b}$ which reduces to

$$\frac{G_b}{C_b} = \frac{G_a}{C_a} \,. \tag{12}$$

Now rewriting Equation (9),

$$Z_{oc} = \frac{1}{G_o + \dfrac{G_b S}{\dfrac{G_b}{C_b} + S} + \dfrac{G_a S}{\dfrac{G_a}{C_a} + S}}$$

and using Equation (12),

$$Z_{oc} = \frac{1}{G_o + \dfrac{G_b S}{\dfrac{G_b}{C_b} + S} + \dfrac{G_a S}{\dfrac{G_b}{C_b} + S}}$$

which reduces to

$$Z_{oc} = \frac{G_b + SC_b}{G_b SC_b + G_a SC_b + G_o SC_b + G_o G_b} \tag{13}$$

Again use $Z_{21T} = \frac{1}{2}(Z_{oc} - Z_{sc})$.

$$Z_{21T} = \frac{1}{2}\left(\frac{G_b + SC_b}{G_b SC_b + G_a SC_b + G_o SC_b + G_o G_b} - \frac{1}{G_o + G_b + SC_a}\right)$$

Rearranging,

$$Z_{21T} = \frac{1}{2} \left(\frac{1}{G_o + G_a + G_b}\right) \left[\frac{S^2 + \frac{G_b^2}{C_a C_b}}{S^2 + S(\theta) + \frac{(G_o G_b)(G_o + G_b)}{(C_a C_b)(G_o + G_a + G_b)}} \right]$$

where $$\theta = \frac{2G_o G_b C_b + G_o G_a C_b + G_o^2 C_b + G_b^2 C_b + G_a G_b C_b + G_o G_b C_a}{(C_a C_b)(G_o + G_a + G_b)}$$

Z_{21T} is now seen to have the basic form

$$\frac{S^2 + \omega_o^2}{S^2 + S\frac{\omega_o}{Q_o} + \omega_o^2} .$$

To obtain Z_{21T} in exactly this form the following relationships must hold:

$$C_a C_b \omega_o^2 = G_b^2 = \frac{(G_o G_b)(G_o + G_b)}{(G_o + G_a + G_b)} \tag{14}$$

and

$$\frac{\omega_o}{Q_o} = \frac{2G_o G_b C_b + G_o G_a C_b + G_o^2 C_b + G_b^2 C_b + G_a G_b C_b + G_o G_b C_a}{C_a C_b (G_o + G_a + G_b)} \tag{15}$$

Solving Equation (14) for G_b and requiring that G_b always be positive,

$$G_b = \frac{-G_a + \sqrt{G_a^2 + 4G_o^2}}{2} \tag{16}$$

Using Equation (15) and $\omega_o = G_b/\sqrt{C_a C_b}$,

$$Q_o = \frac{\sqrt{C_a C_b}\ (G_b)(G_o + G_a + G_b)}{2G_o G_b C_b + G_o G_a C_b + G_o^2 C_b + G_b^2 C_b + G_o G_b C_b + G_o G_b C_a} \tag{17}$$

It will be useful to have all circuit elements in the parallel-T given in terms of one circuit element such as G_o. First, consider Equation (16) where

$$G_b = \frac{-G_a + \sqrt{G_a^2 + 4G_o^2}}{2} \tag{16}$$

If G_a is given as a function of G_b Equation (16) can be solved for G_b as a function of G_o. This can be accomplished by letting $G_a = nG_b$ where n must be greater than zero. Solving Equation (16) for G_b there results

$$G_b = \frac{G_o}{\sqrt{n+1}} \tag{18}$$

and

$$G_a = nG_b = \frac{nG_o}{\sqrt{n+1}} \tag{19}$$

Also, from Equation (12) it can be seen that $C_a = nC_b$. Using this relationship and $\omega_o = G_b/\sqrt{C_a C_b}$ it can be written that

$$C_b = \frac{G_o}{\sqrt{n(n+1)}\ \omega_o} \tag{20}$$

and

$$C_a = nC_b = \frac{nG_o}{\sqrt{n(n+1)}\ \omega_o} \tag{21}$$

Substituting Equations (18),(19),(20) and (21) into Equation (17) for Q_o it can be written that

$$Q_o = \frac{\sqrt{n(n+1)}}{2(n+1)} \tag{22}$$

The choice of an actual value for n must be given special consideration and this will be discussed later. The transfer impedance can now be rewritten as

$$Z_{21T} = \frac{1}{2G_o(1+\sqrt{n+1})}\left(\frac{S^2+\omega_o^2}{S^2+S\frac{\omega_o}{Q_o}+\omega_o^2}\right)$$

Dividing numerator and denominator by ω_o^2 and letting $\rho = \omega/\omega_o$ there results

$$Z_{21T} = \frac{1}{2G_o(1+\sqrt{n+1})}\left(\frac{1-\rho^2}{(1-\rho^2)+j(\frac{\rho}{Q_o})}\right) \tag{23}$$

and

$$2G_o\,|Z_{21T}| = \frac{1}{(1+\sqrt{n+1})}\sqrt{\frac{1}{1+4(\frac{n+1}{n})\left(\frac{\rho}{1-\rho^2}\right)^2}} \tag{24}$$

Equation (24) is plotted in Figure 11 for several values of n.

Also, it will be important to consider the phase shift produced by the parallel-T feedback network. This phase shift will be represented by φ where

$$Z_{21T} = |Z_{21T}| \angle\varphi$$

From Equations (22) and (23) it can be written that

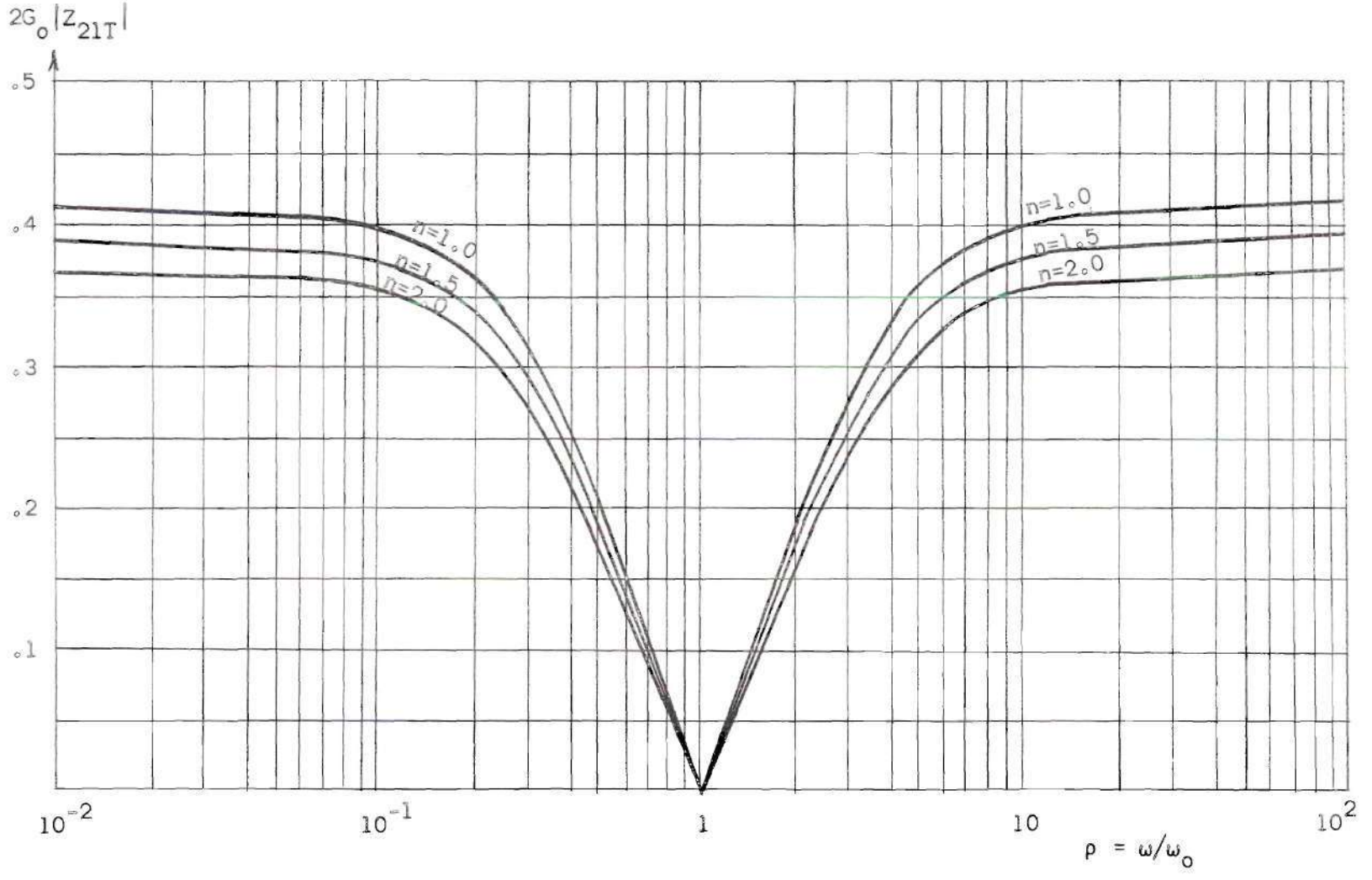


Figure 11. Parallel-T Transfer Impedance.

$$\varphi = -\mathrm{Tan}^{-1}\left[2\sqrt{\frac{n+1}{n}}\left(\frac{\rho}{1-\rho^2}\right)\right] \qquad (25)$$

φ in Equation (25) is plotted in Figure 12 for several values of n.

Now consider the driving point impedance Z_{11T} for the parallel-T. Recall that

$$Z_{11T} = \frac{1}{2}\left(Z_{oc} + Z_{sc}\right)$$

Using Equations (10) and (13)

$$Z_{11T} = \frac{1}{2}\left(\frac{G_b + SC_b}{G_bSC_b + G_aSC_b + G_oSC_b + G_oG_b} + \frac{1}{G_o + G_b + G_a}\right)$$

With some manipulation there results

$$Z_{11T} = \frac{1}{2}\left(\frac{1}{G_o + G_a + G_b}\right)\left[\frac{S^2 + S(\delta) + \dfrac{(G_b)(G_b + 2G_o)}{C_aC_b}}{S^2 + S(\Delta) + \dfrac{(G_oG_b)(G_o + G_b)}{(C_aC_b)(G_o + G_a + G_b)}}\right]$$

where $$\delta = \frac{2G_oC_b + 2G_bC_b + G_bC_a + G_aC_b}{C_aC_b}$$

$$\Delta = \frac{2G_oG_bC_b + G_oG_aC_b + G_o^2C_b + G_b^2C_b + G_aG_bC_b + G_oG_bC_a}{(C_aC_b)(G_o + G_a + G_b)}$$

and using Equations (18), (19), (20), and (21)

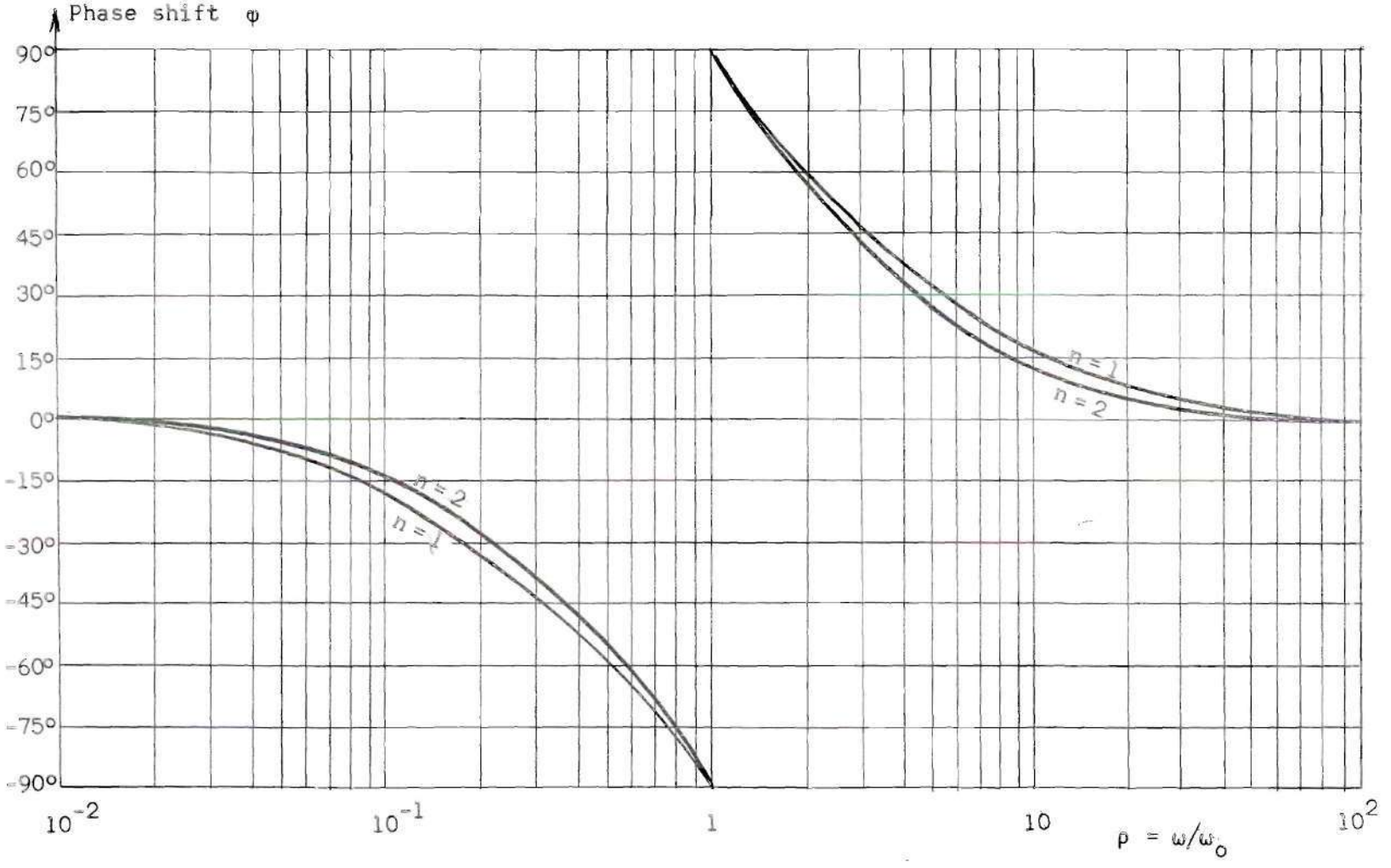


Figure 12. Phase Shift Associated with Transfer Impedance for Parallel-T.

$$Z_{11T} = \frac{1}{2G_o(1+\sqrt{n+1})}\left[\frac{s^2 + s\left(\frac{2\omega_o(\sqrt{n+1}+n+1)}{\sqrt{n}}\right) + \omega_o^2(1+2\sqrt{n+1})}{s^2 + s\frac{\omega_o}{Q_o} + \omega_o^2}\right] \quad (26)$$

Load Circuit

The transfer and driving point impedances for the load circuit will now be derived. The transfer impedance will be considered first and it will be derived to correspond with Equation (4).

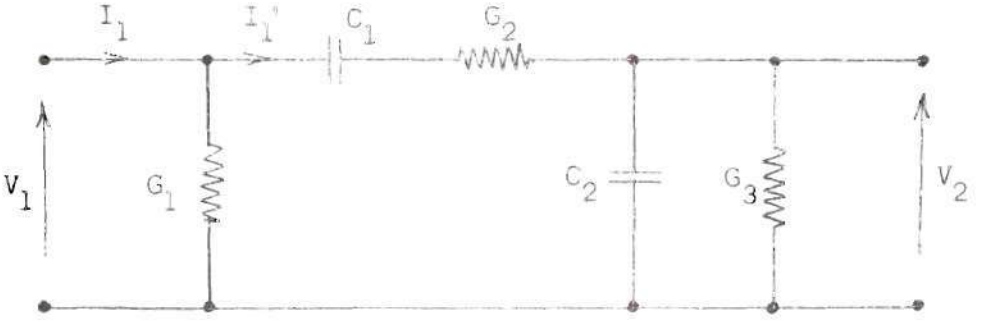


Figure 13. Load Circuit.

With reference to Figure 13

$$Z_{21L} = V_2/I_1$$

$$V_2 = I_1'\left(\frac{1}{G_3 + SC_2}\right)$$

and

$$I_1' = \frac{I_1\left(\frac{1}{G_1}\right)}{\left(\frac{1}{G_1} + \frac{SC_1 + G_2}{G_2SC_1} + \frac{1}{SC_2 + G_3}\right)}$$

$$Z_{21L} = \frac{V_2}{I_1} = \frac{\frac{1}{G_1}\left(\frac{1}{SC_2 + G_3}\right)}{\left(\frac{1}{G_1} + \frac{SC_1 + G_2}{C_2SC_1} + \frac{1}{SC_2 + G_3}\right)}$$

Rearranging

$$Z_{21L} = \frac{G_2}{C_2(G_1+G_2)}\left[\frac{S}{S^2 + S\left(\frac{G_2G_3C_1+G_1G_2C_2+G_1G_3C_1+G_1G_2C_1}{(C_1C_2)(G_1+G_2)}\right) + \frac{G_1G_2G_3}{C_1C_2(G_1+G_2)}}\right]$$

Recall that the desired form for Z_{21L} here is

$$\frac{S}{S^2 + S\frac{\omega_o}{Q_o} + \omega_o^2}$$

Hence it can be written that

$$\frac{\omega_o}{Q_o} = \frac{G_2G_3C_1 + G_1G_2C_2 + G_1G_3C_1 + G_1G_2C_2}{C_1C_2(G_1 + G_2)}$$

and

$$\omega_o = \sqrt{\frac{G_1G_2G_3}{C_1C_2(G_1 + G_2)}}$$

Also,

$$Q_o = \frac{\sqrt{G_1G_2G_3C_1C_2(G_1 + G_2)}}{G_2G_3C_1 + G_1G_2C_2 + G_1G_3C_1 + G_1G_2C_1}$$

Thus

$$Z_{21L} = \frac{G_2}{C_2(G_1 + G_2)} \left(\frac{S}{S^2 + S\frac{\omega_o}{Q_o} + \omega_o^2} \right)$$

Now consider the driving point impedance for the load circuit. With reference to Figure 13

$$Z_{11L} = \frac{V_1}{I_1}$$

$$Z_{11L} = \frac{1}{G_1 + \frac{1}{\frac{1}{G_2} + \frac{1}{SC_1} + \frac{1}{G_3 + SC_2}}}$$

which reduces to

$$Z_{11L} = \frac{1}{G_1+G_2} \left[\frac{S^2 + S\left(\frac{G_3C_1 + G_2C_2 + G_2C_1}{C_1C_2}\right) + \frac{G_2G_3}{C_1C_2}}{S^2 + S\left(\frac{G_1G_3C_1+G_1G_2C_2+G_1G_2C_1+G_2G_3C_1}{C_1C_2(G_1 + G_2)}\right) + \frac{G_1G_2G_3}{C_1C_2(G_1 + G_2)}} \right] \quad (27)$$

Parallel Combination of Load and Feedback Circuits

It will be useful to know the impedance magnitude of the load in parallel with the parallel-T feedback network. This impedance will be seen by the last amplifying stage and will give the slope of the major axis of the elliptical dynamic path for this stage as illustrated in Figure 14.

The driving point impedance for the parallel-T network can be rewritten from Equation (26) as

$$Z_{11T} = \frac{1}{2G_o(1 + \sqrt{n+1})} \left[\frac{\left(\omega_o^2(1 + 2\sqrt{n+1}) - \omega^2\right) + j\omega\omega_o\left(\frac{2(\sqrt{n+1} + n + 1)}{\sqrt{n}}\right)}{(\omega_o^2 - \omega^2) + j\omega\omega_o\left(2\sqrt{\frac{n+1}{n}}\right)} \right]$$

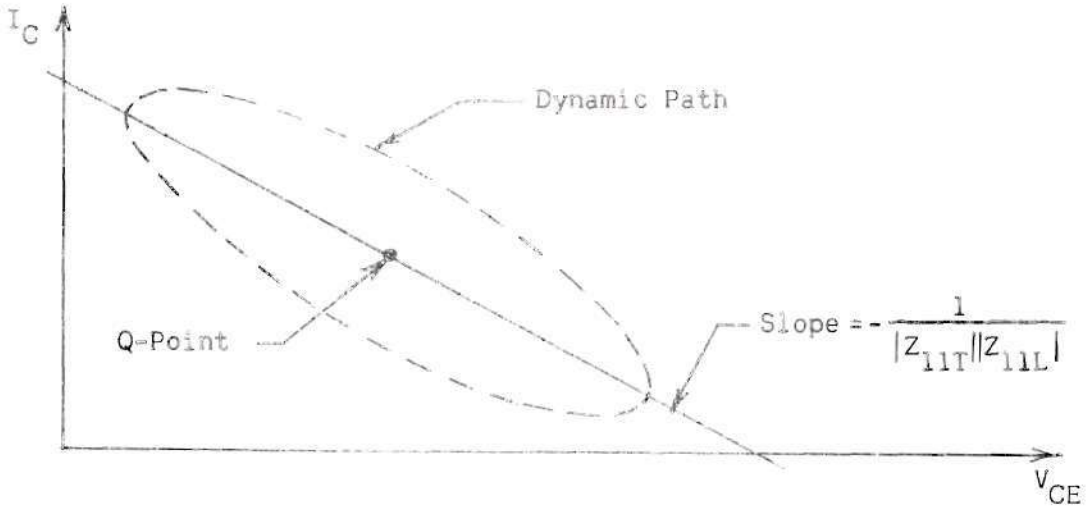


Figure 14. Dynamic Operating Path Determined by Load in Parallel with Feedback Network.

Now divide numerator and denominator by ω_o^2 and let $\rho = \omega/\omega_o$ so that

$$Z_{11T} = \frac{1}{2G_o(1+\sqrt{n+1})}\left[\frac{\left((1+2\sqrt{n+1})-\rho^2\right)+j\rho\left(\frac{2(\sqrt{n+1}+n+1)}{\sqrt{n}}\right)}{(1-\rho^2)+j\rho\left(2\sqrt{\frac{n+1}{n}}\right)}\right]$$

and

$$|Z_{11T}| = \frac{1}{2G_o(1+\sqrt{n+1})}\sqrt{\frac{\left((1+2\sqrt{n+1})-\rho^2\right)^2+\frac{4\rho^2}{n}(\sqrt{n+1}+n+1)^2}{(1-\rho^2)^2+4\rho^2\left(\frac{n+1}{n}\right)}}$$

Recalling that $Z_{11T} = KZ_{11L}$ it can be shown that

$$|Z_{11T}||Z_{11L}| = \frac{|Z_{11T}|}{(K+1)}$$

and it can be written that

$$2(K+1)G_o|Z_{11T}||Z_{11L}| = \frac{1}{(1+\sqrt{n+1})}\sqrt{\frac{\left((1+2\sqrt{n+1})-\rho^2\right)^2+\frac{4\rho^2}{n}(\sqrt{n+1}+n+1)^2}{(1-\rho^2)^2+4\rho^2(\frac{n+1}{n})}} \quad (28)$$

Equation (28) is plotted in Figure 15 for several values of n.

Load Circuit Elements as a Function of K and G_o

All circuit elements in the parallel-T network have been given in terms of G_o. It will prove useful to now give all load circuit elements as a function of K and G_o.

Recall Equation (5) which is restated here as $Z_{11T} = KZ_{11L}$. Using Z_{11T} from Equation (26) and Z_{11L} from Equation (27) it can be written that

$$\frac{1}{2G_o(1+\sqrt{n+1})}\left[\frac{s^2+s\left(\frac{2(\sqrt{n+1}+n+1)}{\sqrt{n}}\right)+\omega_o^2(1+2\sqrt{n+1})}{s^2+s\frac{\omega_o}{Q_o}+\omega_o^2}\right]$$

$$=\frac{K}{G_1+G_2}\left[\frac{s^2+s\left(\frac{G_3C_1+G_2C_2+G_2C_1}{C_1C_2}\right)+\frac{G_2G_3}{C_1C_2}}{s^2+s\left(\frac{G_1G_3C_1+G_1G_2C_2+G_1G_2C_1+G_2G_3C_1}{C_1C_2(G_1+G_2)}\right)+\frac{G_1G_2G_3}{C_1C_2(G_1+G_2)}}\right] \quad (29)$$

From Equation (29) the following is evident:

$$\frac{K}{G_1+G_2} = \frac{1}{2G_o(1+\sqrt{n+1})}$$

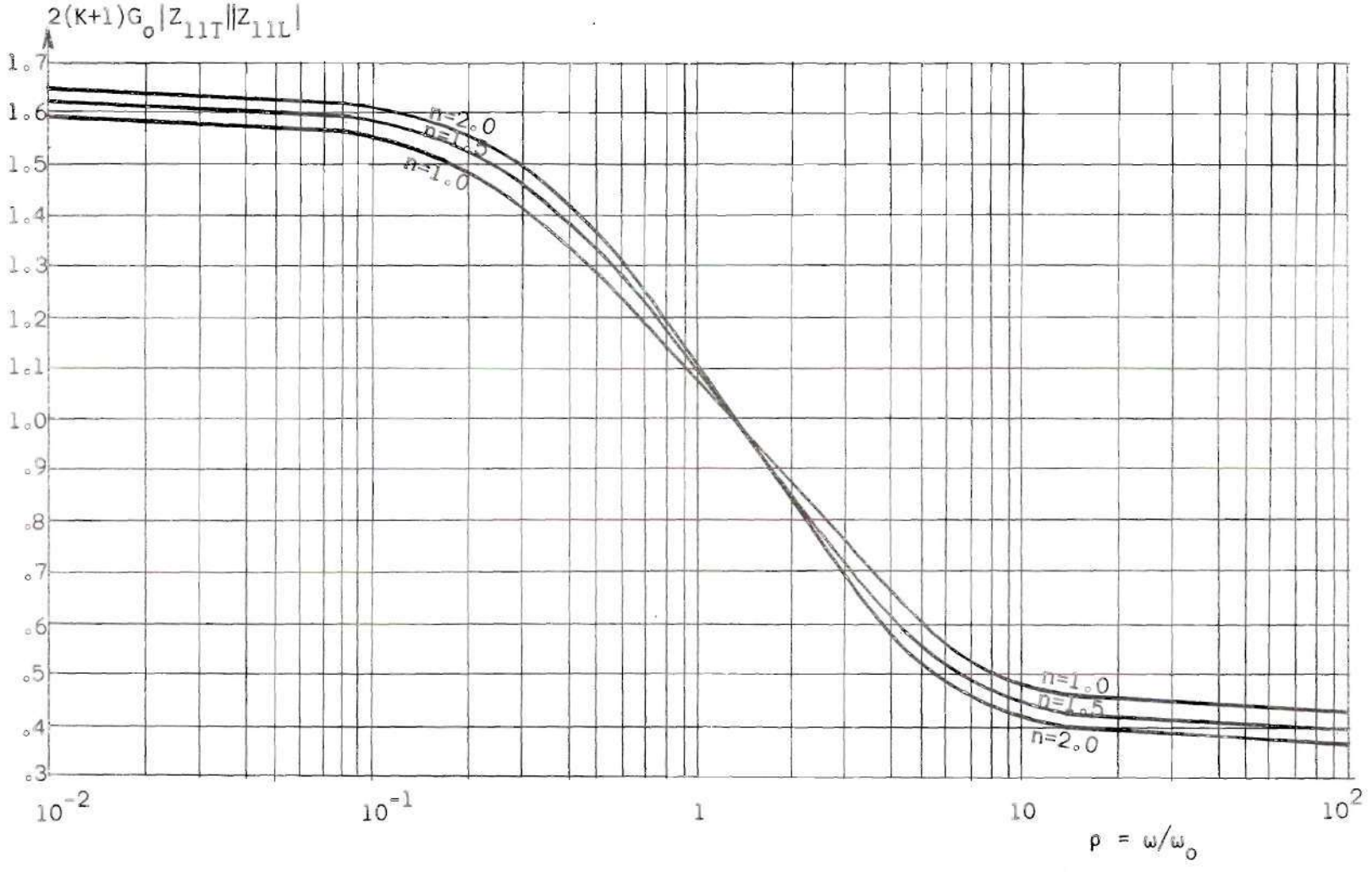


Figure 15. Impedance Magnitude for Load in Parallel with Parallel-T.

$$\frac{G_3C_1 + G_2C_2 + G_2C_1}{C_1C_2} = \frac{2\omega_o(\sqrt{n+1} + n + 1)}{\sqrt{n}}$$

$$\frac{G_2G_3}{C_1C_2} = \omega_o^2(1 + 2\sqrt{n+1})$$

$$\frac{G_1G_3C_1 + G_1G_2C_2 + G_1G_2C_1 + G_2G_3C_1}{C_1C_2(G_1 + G_2)} = \frac{\omega_o}{Q_o}$$

$$\frac{G_1G_2G_3}{C_1C_2(G_1 + G_2)} = \omega_o^2$$

Solving for G_1, G_2, G_3, C_1 and C_2 it can be written that

$$G_1 = 2KG_o\left(\frac{1 + \sqrt{n+1}}{1 + 2\sqrt{n+1}}\right) \tag{30}$$

$$G_2 = 2G_1\sqrt{n+1} \tag{31}$$

$$C_1 = \frac{4KG_o}{\omega_o}\sqrt{\frac{n+1}{n}}\left(\frac{1 + \sqrt{n+1}}{1 + 2\sqrt{n+1}}\right)\left(1 - \frac{1 + \sqrt{n+1}}{1 + 2\sqrt{n+1}}\right) \tag{32}$$

$$C_2 = \frac{nC_1G_2^2}{2C_1G_2\omega_o\sqrt{n}\ (\sqrt{n+1} + n + 1) - nC_1^2\omega_o^2(1+2\sqrt{n+1}) - nG_2^2} \tag{33}$$

$$G_3 = \frac{C_1C_2\omega_o^2(1 + 2\sqrt{n+1})}{G_2} \tag{34}$$

It is obvious that once K, G_o, and n are decided upon all five circuit elements in the load circuit can be determined from Equations (30), (31), (32), (33), and (34).

Determination of Optimum n and Circuit Elements

The choice of the parameter n will have a profound effect on the overall circuit operation. Therefore, a procedure for determining the best n will now be presented.

From Equation (8), where the overall circuit Q-factor was given as

$$Q = Q_o(1 + \beta K_o) ,$$

it can be seen that the K_oQ_o product should be maximized for best results. Recall from Equation (7) that

$$K_o = \frac{g_m k}{2} \left(\frac{1}{G_o + G_a + G_b} \right)$$

or after substituting Equations (18) and (19)

$$K_o = \frac{g_m k}{2G_o(1 + \sqrt[4]{n+1})}$$

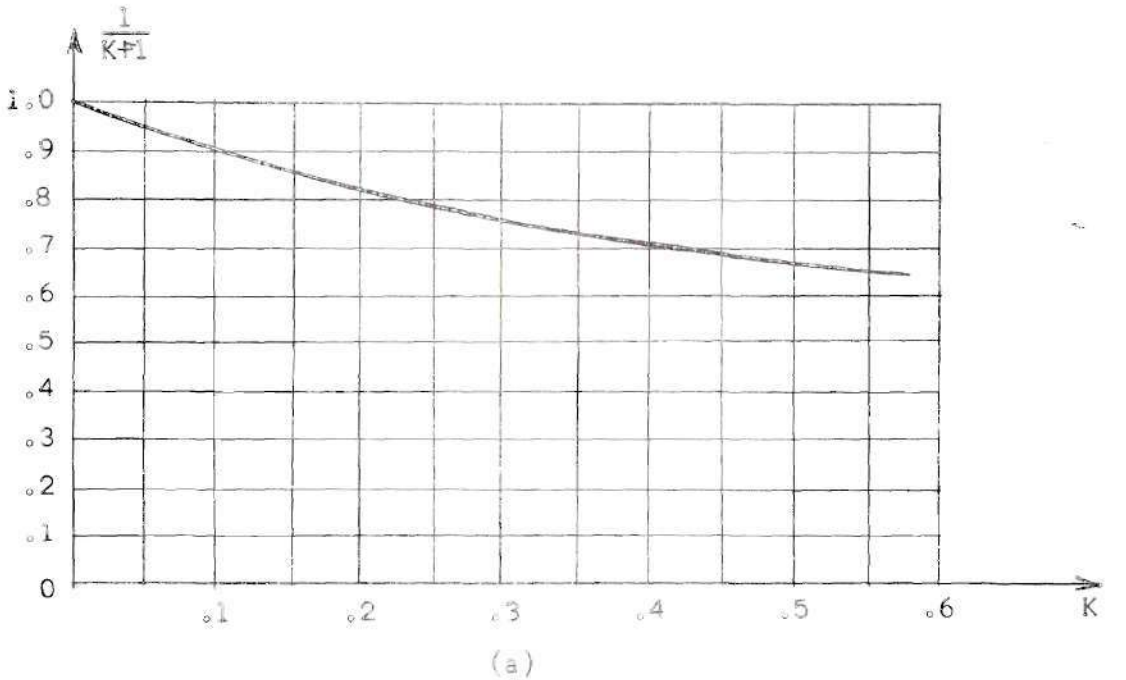
Using Q_o from Equation (22), the K_oQ_o product is

$$K_oQ_o = \frac{g_m k \sqrt[4]{n}}{4G_o(\sqrt[4]{n+1} + n + 1)} = \frac{g_m \sqrt[4]{n}}{4(K+1)G_o(\sqrt[4]{n+1} + n + 1)}$$

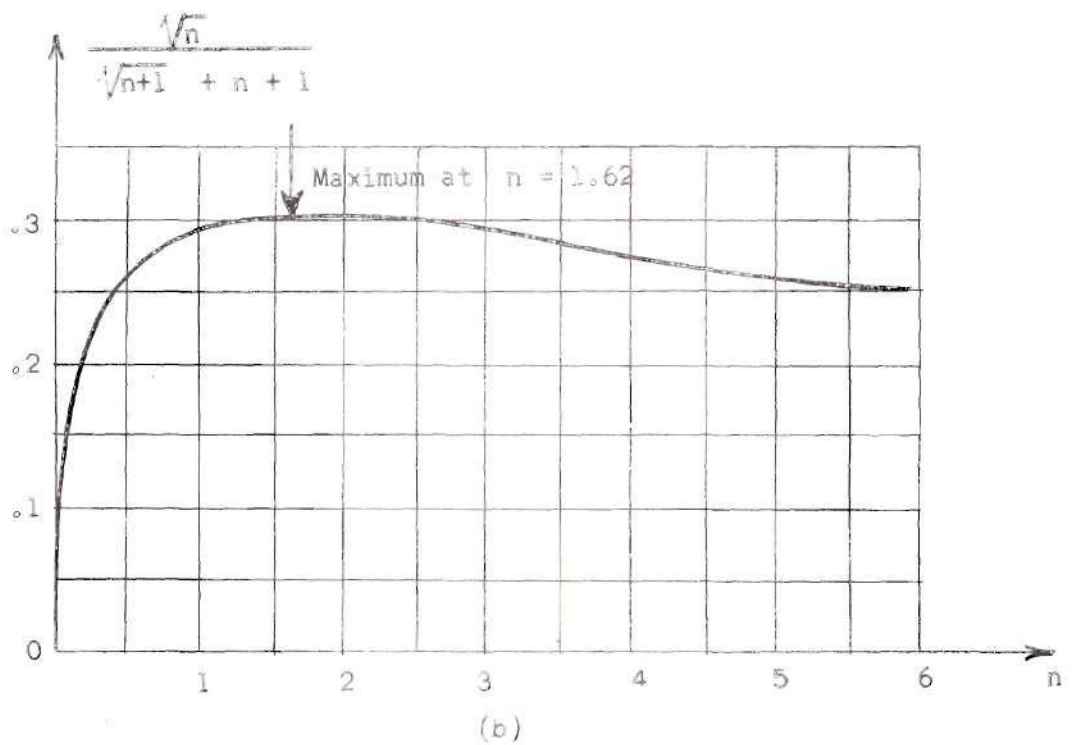
or K_oQ_o is proportional to

$$\frac{1}{G_o} \circ \frac{1}{K+1} \circ \frac{\sqrt[4]{n}}{\sqrt[4]{n+1} + n + 1} \qquad (35)$$

Figure 16a is a plot of $1/K+1$ and Figure 16b is a plot of

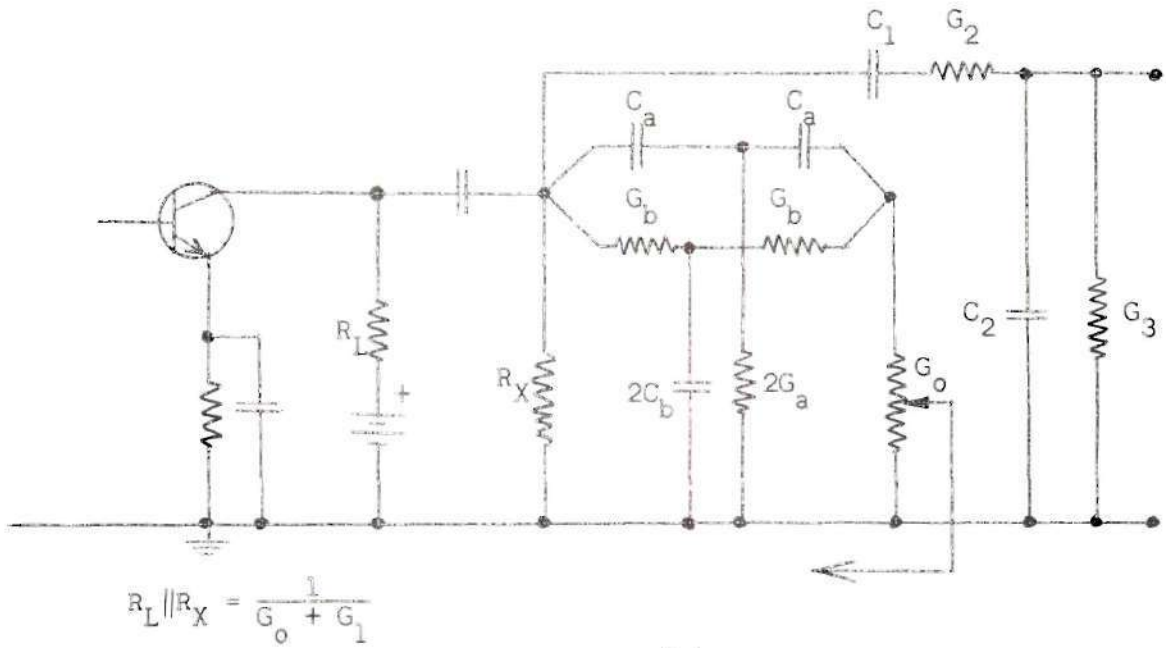


(a)

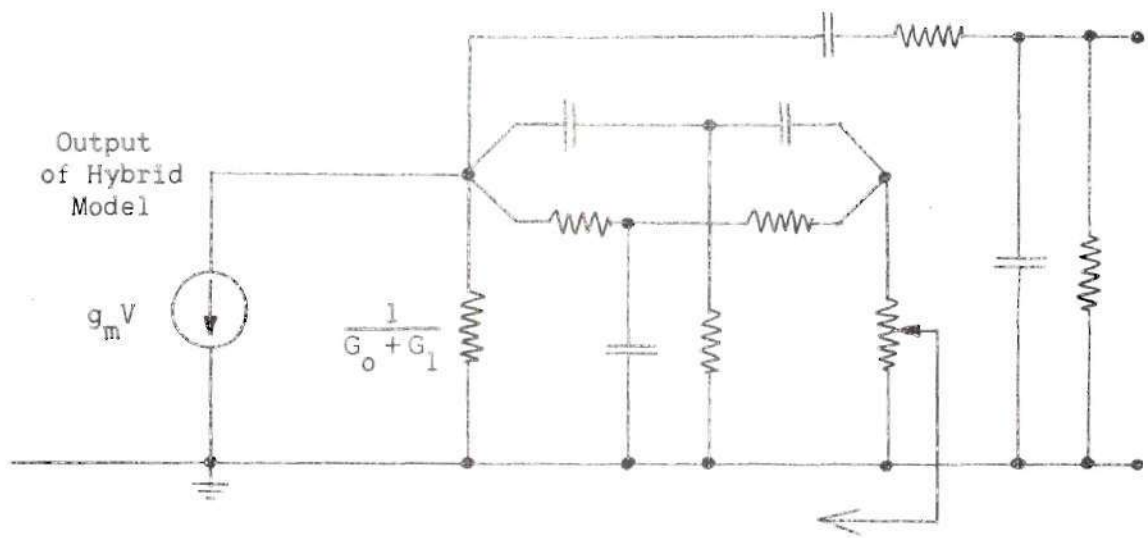


(b)

Figure 16. Relative Magnitude of $K_o Q_o$.



(a)



(b)

Figure 17. Last Transistor Stage Coupled with Load and Feedback Circuits.

$$\frac{\sqrt{n}}{\sqrt{n+1} + n + 1}$$

n must be greater than zero because of the way in which it was defined. Although the curve in Figure 16b indicates that $n \sim 1.62$ might best maximize $K_o Q_o$, other criteria must also be considered in determining n:

(a) $1/G_o$ must be at least ten times smaller than the impedance loading the parallel-T's output.

(b) The d.c. load resistance on the last transistor stage must be greater than or equal to $1/G_o+G_1$. i.e. $R_L \geq \frac{1}{G_o + G_1}$. This requirement must be met so that $R_L \| R_X$ in Figure 17a can be made equal to $1/G_o+G_1$. Now a voltage controlled current source, Figure 17b, will feed the parallel combination of the load circuit and the parallel-T as in the theoretical analysis pertaining to Figure 9.

(c) $|Z_{11T} \| Z_{11L}|$ must present a satisfactory a.c. load to the last amplifying stage.

(1) The dynamic operating path must lie within the maximum voltage, current and power ratings for the transistor used. See Figure 18.

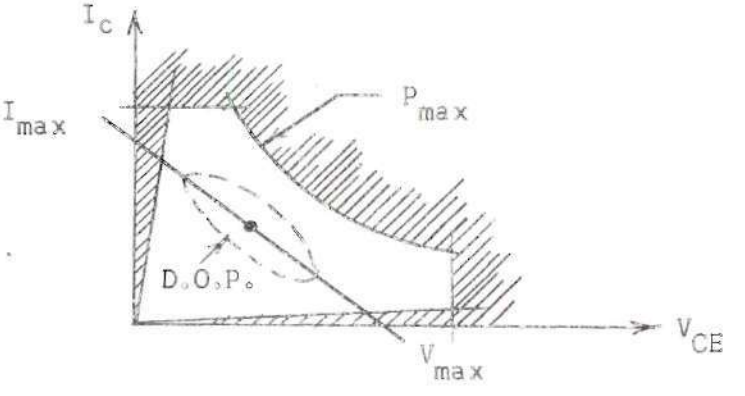


Figure 18. Allowed Operating Region on Transistor Characteristics.

(2) It will be desired, for noise considerations, that a large voltage swing be possible on the output of the last stage. However, this voltage swing should not be so large that signal distortion occurs.

(3) The a.c. load should not be so large that the last stage ceases to operate as a constant current feeding a load.

Whether the a.c. load presented to the output of a stage is satisfactory can, of course, only be determined after the transistors are chosen.

The procedure for determining n will be to maximize K_oQ_o in Equation (35) by considering each of the three terms in the product. However, the requirements listed above must be met in the process of maximizing K_oQ_o. n can be decided upon by the following procedure:

(a) Choose K to be some small value. Refer to Figure 16a and try to make 1/K+1 large because of its effect on Equation (35).

(b) Decide how large the impedance can be into which the parallel-T operates. This impedance should be made as large as possible, but will have certain physical limitations which will be discussed in Chapter III.

(c) Choose $1/G_o$ as large as possible but at least ten times less than the impedance loading the parallel-T's output. $1/G_o$ should be made as large as possible because of its effect on Equation (35). Also, it will simplify matters to choose $1/G_o$ to be a commercially available potentiometer.

(d) Choose n, preferably between 1.0 and 2.5, and refer to Figure 15 to determine $|Z_{11T}||Z_{11L}|$. Also, using Equation (30), it can be written that

$$R_L \text{ on last stage} \geq \frac{1}{G_o + G_1} = \frac{1}{G_o\left(1 + 2K\left(\frac{1 + \sqrt{n+1}}{1 + 2\sqrt{n+1}}\right)\right)}$$

(e) Check to see that all requirements previously discussed are met for the particular transistors to be used. If not, either change the choice of parameters or the choice of transistors.

(f) All circuit elements in the parallel-T can be calculated from Equations (18), (19), (20), and (21). All circuit elements in the load circuit can be calculated from Equations (30), (31), (32), (33), and (34).

CHAPTER III

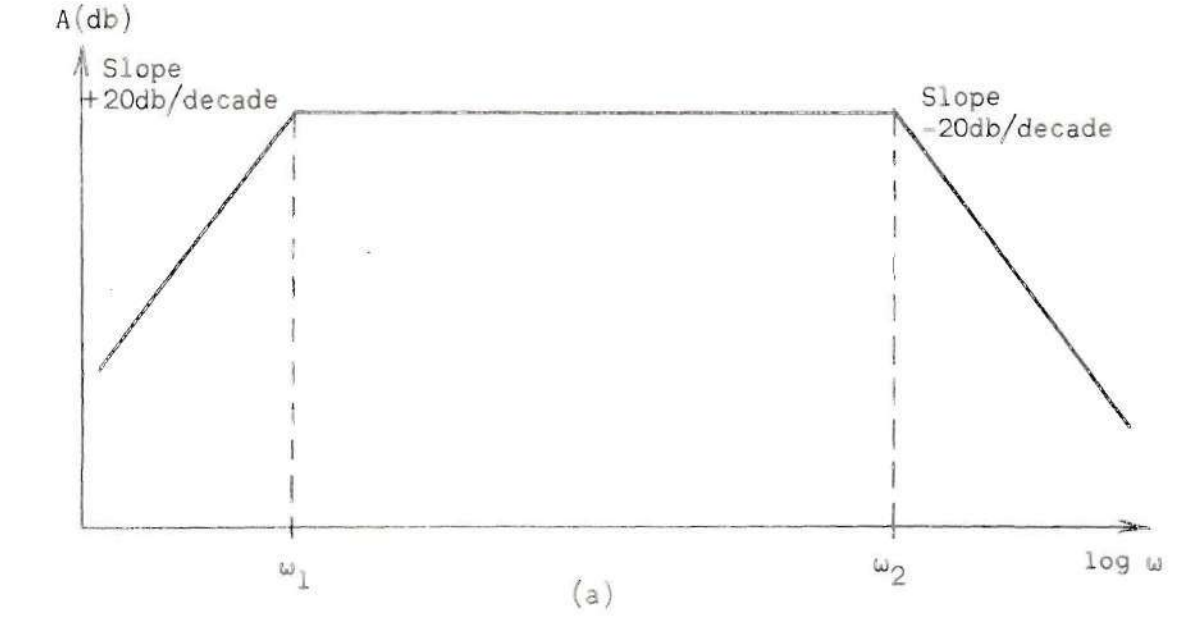
CIRCUIT DESIGN

Amplifier Requirements

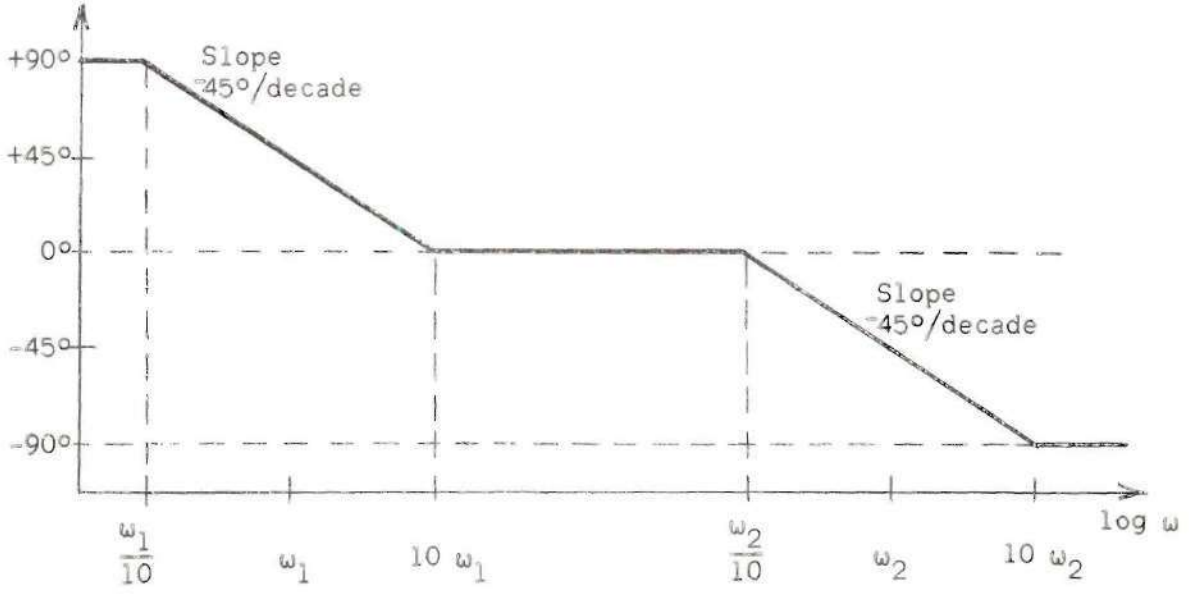
Transistor amplifiers will provide the voltage gain necessary for operation of the proposed circuit. The number of stages required will depend on the maximum overall $Q = Q_{max}$ desired, the type amplifiers used, and other factors. The proposed circuit will be designed for a center frequency $f_o = 1$ kc/s and $Q_{max} \sim 500$.

The general requirement for stability in a feedback amplifier is that the closed loop voltage gain reaches 0 db before the phase shift around the loop reaches 180°. If this requirement is met, the feedback is known as negative or degenerative feedback. This stability requirement must be given special consideration in the design of the amplifier section of the proposed circuit.

It will now be beneficial to review the basic rules relating the logarithmic amplitude and phase characteristics for the amplifiers to be used. For the present it will be quite satisfactory to consider only the asymptotes of the characteristics. Figure 19a is the asymptotic frequency response for a single stage amplifier which has a high and low cutoff frequency of ω_2 and ω_1 respectively. The term "cutoff" refers to the points where the actual characteristic is 3 db down from the mid-band gain. At the cutoff frequencies the voltage gain in decibels begins to drop off at the rate of 20 db per decade of frequency or 6 db per octave of frequency. As seen in Figure 19b the phase characteristic is also approximated



(a)



(b)

Figure 19. Asymptotic Frequency Response for Single Stage Amplifier.

by straight lines. The phase shift is +90° leading at one decade below the cutoff frequency at the low-frequency end and -90° lagging at one decade above the cutoff frequency at the high-frequency end. At both extremes the phase shift changes at a rate of 45° per decade of frequency.

It will now be assumed that three amplifier stages will be needed to provide sufficient gain and phase reversals in the proposed circuit. This will be found true later if the first stage is a summing amplifier as opposed to a difference amplifier. If only one amplifying stage were to be used the stability problem would be almost nonexistent because the phase shift from the amplifier would never exceed ±90°. However, there would be additional phase shift from the parallel-T network and from parasitic effects, but even with these the overall phase shift could easily be kept under 180° until the closed loop gain had reached 0 db. If two amplifier stages were to be used the amplifier phase shift would approach 180° as a limit at very low and very high frequencies. However, if both stages were common-emitter another phase reversal would be needed. With three amplifying stages the stability problem becomes difficult. It will be instructive to consider the worst possible design where the three stages are identical. In particular, consider the case where all three cut off at 10 kc/s and where the overall voltage gain is 6,250 or 77.8 db. (This voltage gain will later be shown to correspond to $Q_{max} \approx 500$ for $n = 1$, $K = .53$ and $1/G_o = 5K\Omega$.) Figure 20 shows the overall gain and phase shift for the high-frequency cutoff. (It will be assumed that the low-frequency region can be made to meet stability requirements with little difficulty.) From Figure 20 it can be seen that approximately 55 db of

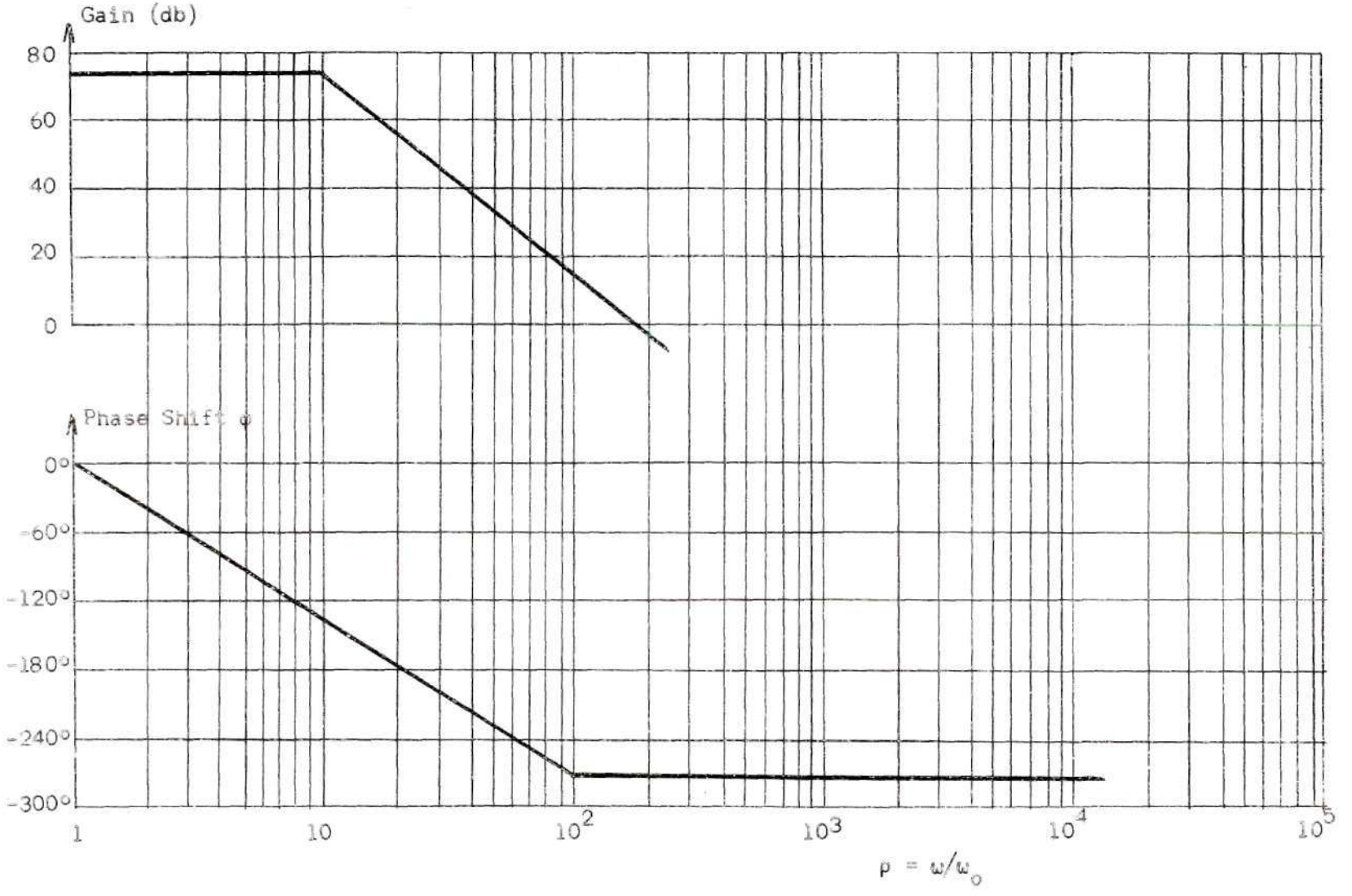


Figure 20. Frequency Response for Three Identical Stages Cutting Off at 10 kc/s.

voltage gain remains when the phase shift reaches 180°. If the proposed circuit were constructed using these three identical stages it would be certain to oscillate long before β was able to reach unity unless some very special phase correction techniques were employed. Recall that $\beta = 1$ corresponds to the overall Q-factor = Q_{max}. The procedure generally recommended for constructing a stable three stage feedback amplifier is to make the bandwidth of two of the stages much greater than that of the third stage. Under these conditions the overall cutoff characteristic is governed primarily by the narrowband stage, for which the phase shift is always less than 90°. In this line of thought let the narrowband stage cut off at 10 kc/s and let both wideband stages cut off at 20 mc/s. This is illustrated in Figure 21. From Figure 21 it can be seen that even for this case about 10 db of gain remains when the phase shift reaches 180° for a mid-band gain of 77.8 db. Also, to construct a two stage wideband (or video) amplifier cutting off at 20 mc/s and meeting other circuit criteria would be difficult. It should now be apparent that the design of a stable three stage feedback amplifier for use in the proposed circuit will require special consideration.

It will suffice to initially think in terms of the unloaded amplifier section and to design it so that its voltage gain reaches 0 db before the phase shift reaches 180°. However, it should be kept in mind that once the amplifier is loaded and the feedback loop is closed through the parallel-T network other phase shifts will be introduced. The additional phase shifts and methods to reduce them will be discussed later.

It is desired that the amplifier's frequency response be centered about $f = f_o$ and that the response be flat in the vicinity of $f_o = 1$ kc/s. Exactly how wide the amplifier's response should be can be determined only

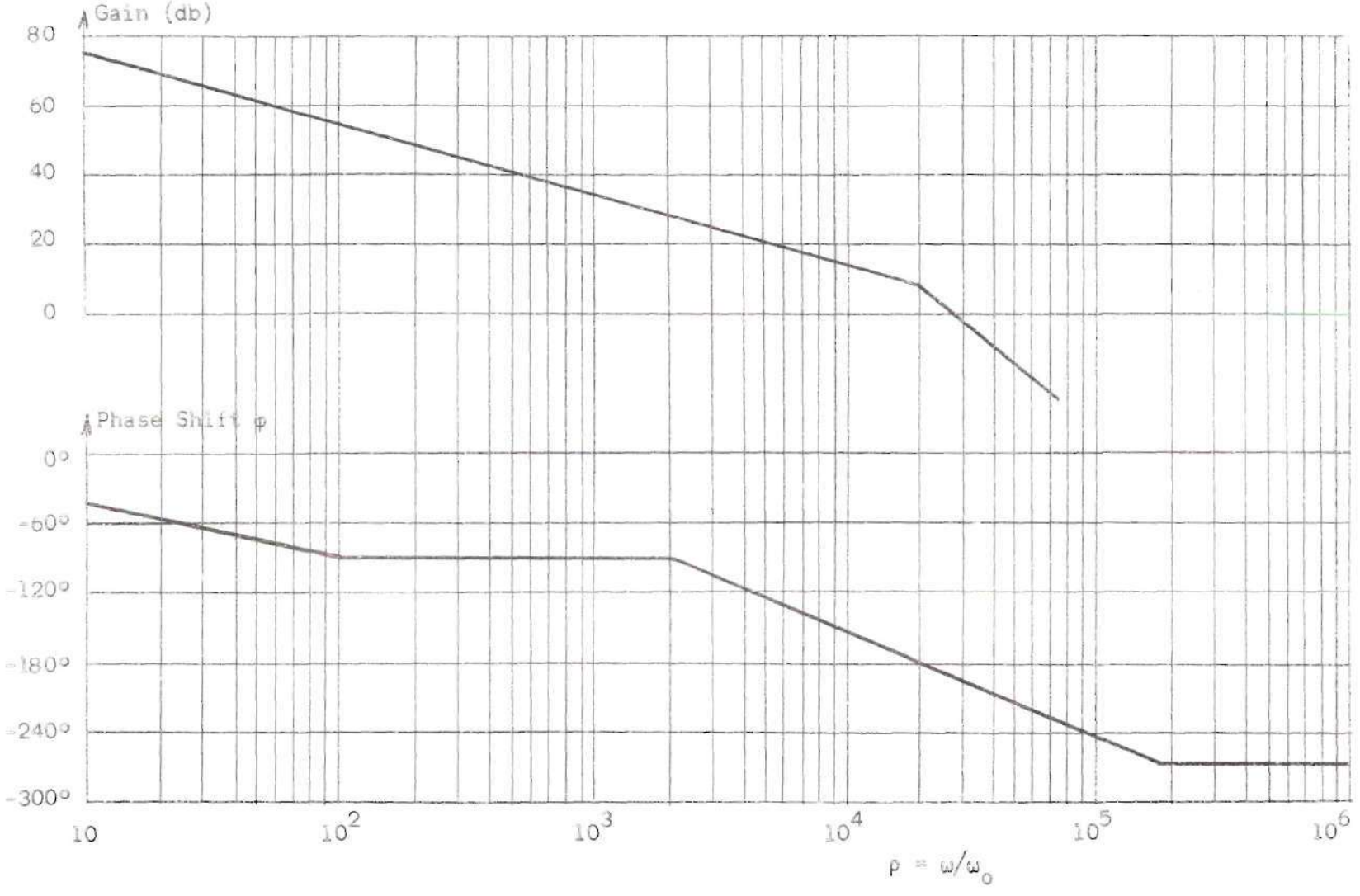


Figure 21. Frequency Response for One Stage Cutting Off at 10 kc/s and Two Stages at 20 mc/s.

after $Q_o = f(n)$ is decided upon. Recall that the overall $Q = Q_o(1 + \beta K_o)$ and for $\beta = 0$ it can be written that $Q = Q_o$. The overall bandwidth involved here is given by

$$B.W. = \frac{f_o}{Q} = \frac{f_o}{Q_o}$$

Note that $\beta = 0$, or $Q = Q_o$, corresponds to the largest bandwidth. It would be best if the amplifier's response were almost flat over the frequency region where the theoretical response, from Equation (8), has any appreciable value for $\beta = 0$. Figure 22 illustrates an amplifier's response relative to the theoretical response for $\beta = 0$. The relative bandwidths shown here should be satisfactory for most any situation since the amplifier's response is flat over the region where the desired overall response has any appreciable value. However, the bandwidth of the amplifier relative to the bandwidth of the equation's response for $Q = Q_o$ can be large or small depending on the intended use of the overall circuit. For example,

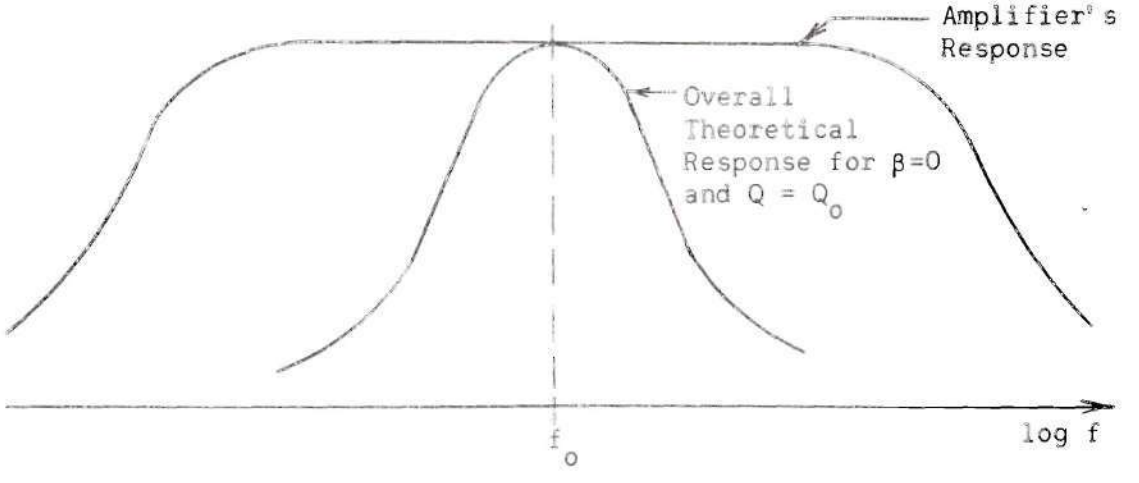


Figure 22. Amplifier Response Relative to Desired Overall Response.

if the circuit was going to be used only for $Q's >> Q_o$ it would not matter much that the overall bandwidth for $Q \sim Q_o$ was lessened by a narrowband amplifier.

Transistor amplifiers are frequency dependent because the parasitic capacitances associated with the transistor and the circuit wiring become important at high frequencies and because bypass and coupling capacitors do not act as short circuits at low frequencies. However, the high frequency cutoff can also be controlled by coupling and bypass capacitors because they will have a profound effect on the value of mid-band gain achieved and there will exist a relationship between the mid-band gain and the bandwidth such that their product will be constant. The result is that it will be possible to construct a high-gain and narrow-bandwidth amplifier or a low-gain and wide-bandwidth amplifier. Figure 23a could be a high-gain transistor amplifier with a narrow-bandwidth and Figure 23b, which is Figure 23a with the emitter bypass capacitor removed, a low-gain wide-bandwidth amplifier. The gain-bandwidth product for both amplifiers

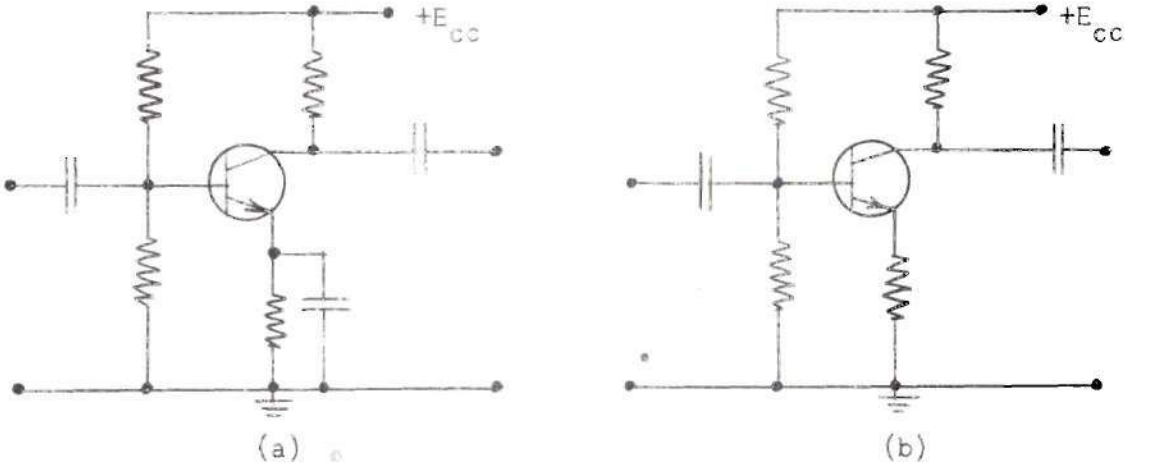


Figure 23. A Low-Gain and a High-Gain Amplifier with Same Gain-Bandwidth Product.

would be the same. Principles such as these will be valuable in designing a stable three stage feedback amplifier.

A possible method for achieving a stable three stage amplifier response with sufficient gain for $Q_{max} \sim 500$ is to use two narrowband stages and one wideband stage. Consider letting the narrowband stages cut off at about 3 kc/s and the wideband stage at about 1 mc/s. Here, the overall response will be governed primarily by the two narrowband stages and the phase shift will reach 180° before the no-load gain reaches 0 db as seen in Figure 24. However, since the phase shift does not go much beyond 180° until the gain has reached 0 db it appears that only a slight phase correction can prevent oscillation once the loop is closed. Also, the narrowband responses can be made to produce an overall response centered at $f_o = 1$ kc/s. Preliminary experimentation has shown that the construction of two stages cutting off at about 3 kc/s and one stage cutting off at about 1 mc/s with the overall response centered near 1 kc/s can be achieved with little difficulty. This general method was the one eventually used.

Input Amplifier and Noise Considerations

The input transistor stage must combine the input voltage with the feedback voltage either by addition or subtraction, provide a high impedance on the output of the parallel-T network, and it must produce a relatively high signal-to-noise ratio at its output so that the noise in the final output of the proposed circuit will not be excessive. The signal to noise ratio for the unloaded amplifier is almost the same as the ratio at the output of the first stage. After the signal and noise leave the first stage they will be amplified by almost the same amount. However, once the load and parallel-T circuits are coupled to the amplifier the noise at the

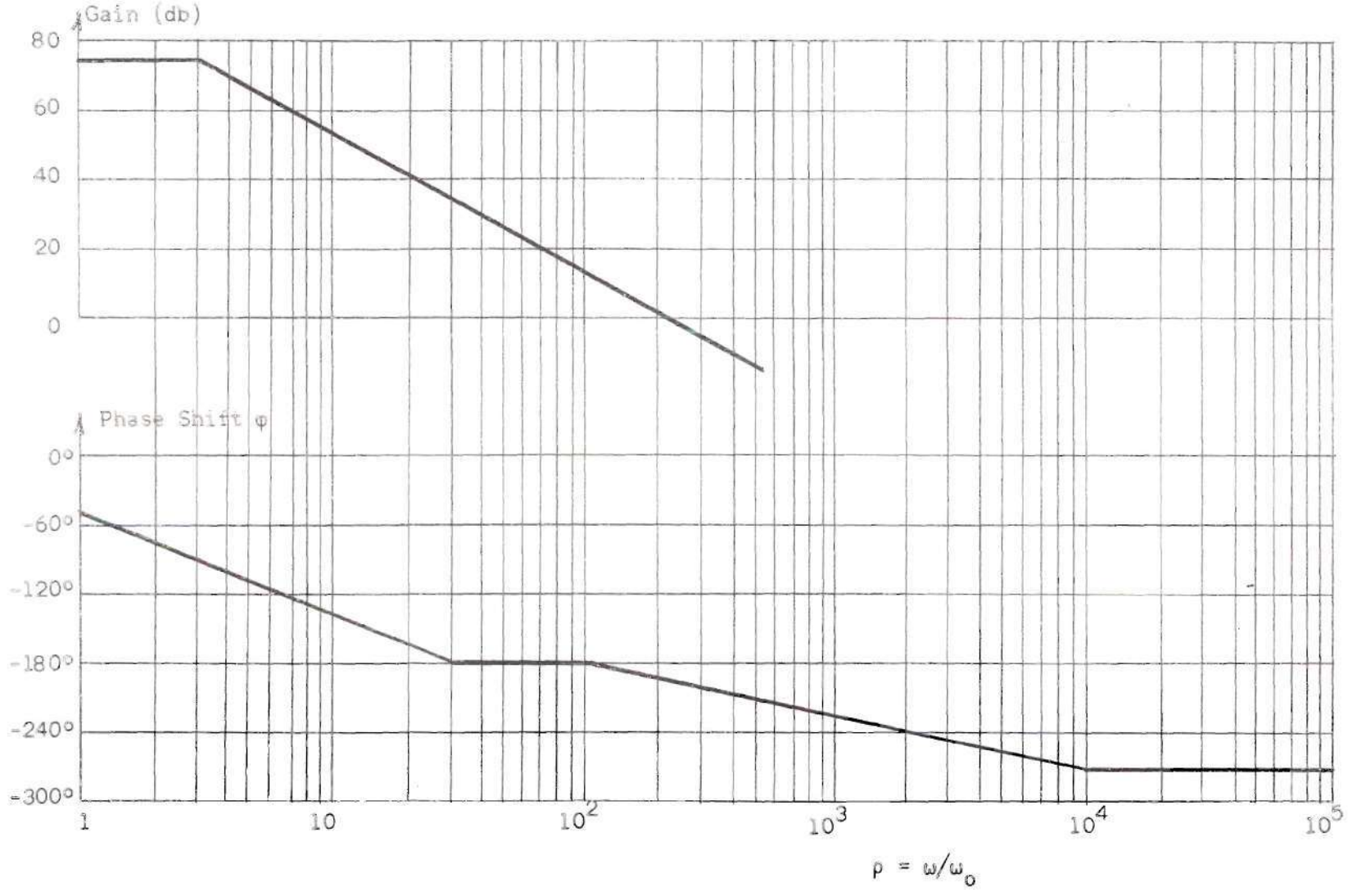


Figure 24. Frequency Response for Two Stages Cutting Off at 3 kc/s and One at 1 mc/s.

output of the load circuit, even for $\beta = 0$, will be less apparent than it had been at the output of the unloaded amplifier. This can be attributed to the fact that the load circuit has a bandpass response that serves to filter out high and low frequency fourier noise components. As β is made greater than zero the negative feedback will eliminate the noise in the output rather quickly. Therefore, the problem is to minimize the load output noise for $\beta = 0$.

There are several ways to increase the signal-to-noise ratio at the output of the first stage as follows:

(a) Use local feedback in the first stage. This could be current feedback or voltage feedback.

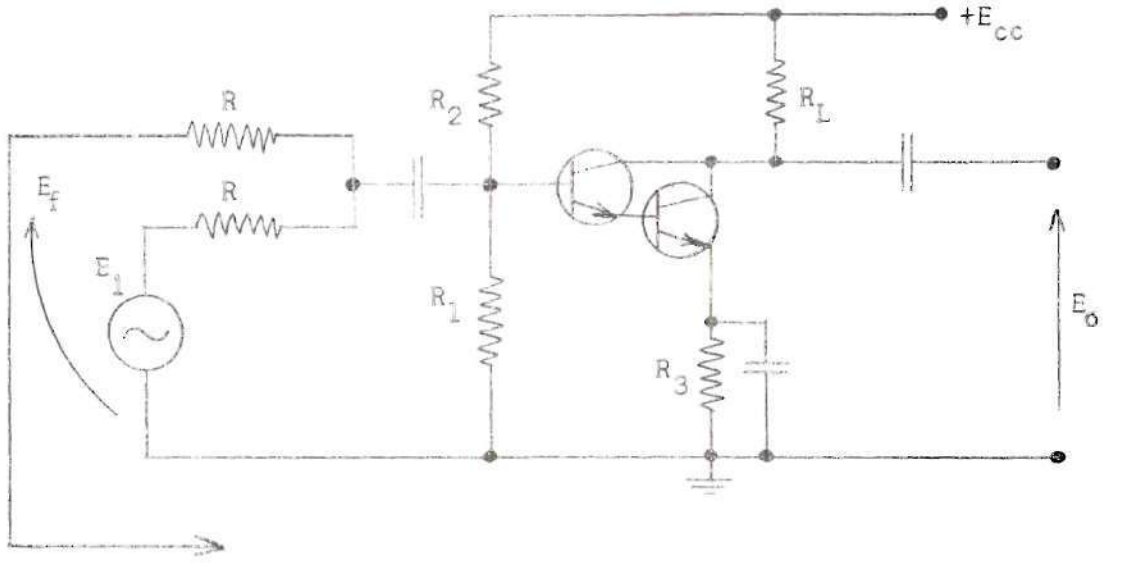
(b) Use local feedback in the second or third stages although it will not have as profound an effect as if used in the first stage.

(c) Allow the first stage to have a large voltage gain.

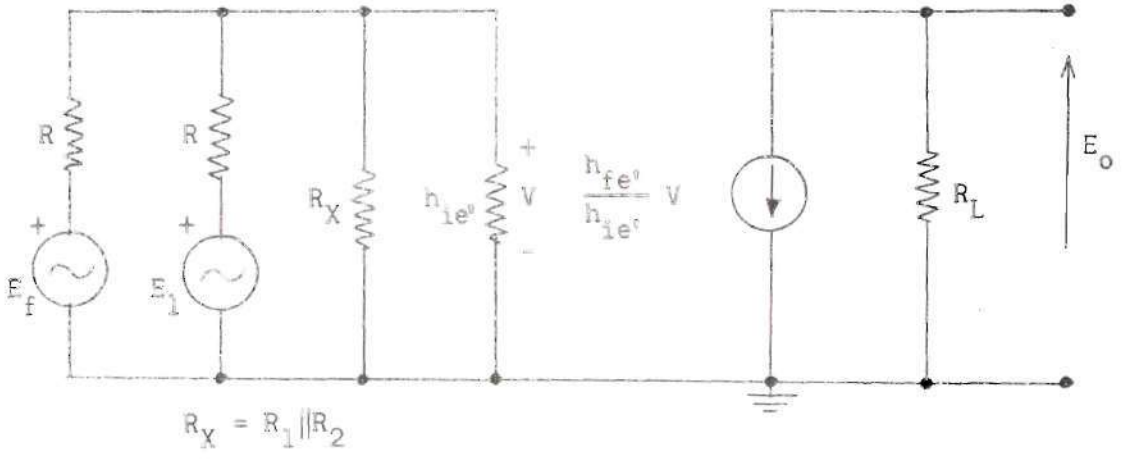
(d) Make the dynamic operating path on the final stage cover a wide voltage range. This allows the input voltage to the first stage to be larger.

The method chosen to increase the signal-to-noise ratio in the first stage will have a definite effect on the frequency response of that stage. Therefore, in designing the first stage the response desired for the overall amplifier must be kept in mind.

For the input transistor stage a summing amplifier is chosen rather than a difference amplifier because the impedance requirement is easier to satisfy with the summing amplifier. Figure 25a shows a possible amplifier for the first stage. It will be instructive to construct a hybrid model for this circuit and derive an equation for e_o to show that summing does



(a)



(b)

Figure 25. Possible Circuit for Summing Amplifier.

indeed occur. Figure 25b is the hybrid model to be used in the analysis. Primes are added to the hybrid parameters to indicate that they are for the transistor compound connection in Figure 25a. From inspection of Figure 25b it can be written that

$$\frac{E_1 - V}{R} + \frac{E_f - V}{R} = \frac{V}{R_X} + \frac{V}{h_{ie'}}$$

or

$$\frac{E_1 + E_f}{R} = V\left(\frac{1}{R_X} + \frac{1}{h_{ie'}} + \frac{2}{R}\right)$$

and

$$V = \frac{E_1 + E_f}{R\left(\frac{1}{R_X} + \frac{1}{h_{ie'}} + \frac{2}{R}\right)}$$

Now $E_o = -\frac{h_{fe'}}{h_{ie'}} VR_L$ or

$$E_o = -\frac{(E_1 + E_f)h_{fe'}R_L}{h_{ie'}R\left(\frac{1}{R_X} + \frac{1}{h_{ie'}} + \frac{2}{R}\right)}$$

This stage will be made to have a high-gain and narrow-bandwidth.

Second and Third Stages

The transistor circuit configuration (i.e. common-base, common-emitter or common-collector) used in each of the three stages will be chosen to satisfy the requirements of the overall circuit. Table 1 will prove quite useful in choosing the circuit configurations.

First, since the input stage is a summing amplifier an odd number

of phase reversals must be provided for stability. Therefore, either one or three phase reversals can be used and a glance at Table 1 will indicate that several possibilities exist. Recall that Figure 25a shows a possible input stage. This stage uses the common-emitter common-emitter compound connection and will have a high input impedance and a fairly high gain. Since this first stage uses a high gain to increase its signal-to-noise ratio it will be desired to preserve this gain once the first stage is coupled to the second stage. This will, of course, require a high input impedance for the second stage and possibly some local feedback in the second stage. Figure 26a shows a circuit with a high input impedance and local current feedback that could be used as the second stage. Also, since the first stage will have a relatively small bandwidth the second stage can easily be made to have a bandwidth on the order of 1 mc/s to qualify as the sole wideband stage. This will require sacrificing gain in the second stage but sufficient gain can be provided by the first and third stages. Note that both the first and second stage produce a phase reversal requiring a phase reversal from the third stage also. In addition, the third stage must have a fairly high voltage gain and a bandwidth on the order of several kilocycles per second to qualify as the other narrowband stage. Figure 26b shows a possible circuit for the third stage. While the compound connection may not be essential for the third stage it does produce a high input impedance to this stage which isolates it and this allows all three stages to be analyzed independently.

It will now be instructive to consider why a three stage amplifier was chosen instead of only one or two stages. It will be shown that a gain of approximately 6000 will be required for $Q_{max} \sim 500$ and experience has

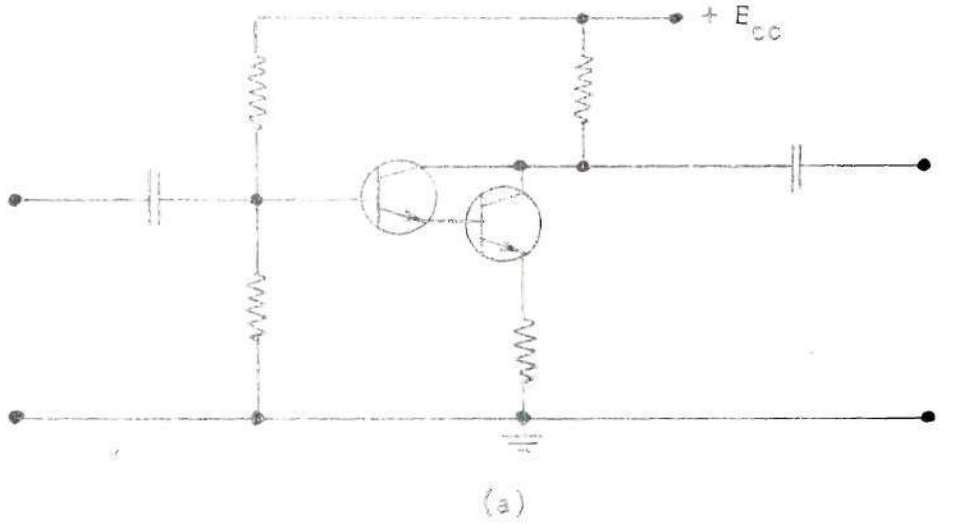
Table 1. Transistor Circuit Configurations and Related Characteristics

	Voltage Gain	Cutoff Frequency	Input Resistance
Common-Emitter (Phase Reversal)	High Gain	$f_{\alpha e} = \frac{f_{\alpha b}}{h_{fe}}$	Moderate Input Resistance ~ 1000 Ω
Common-Base (No Phase Reversal)	High Gain	$f_{\alpha b}$ Highest Cutoff Frequency	Lowest Input Resistance ~ 50 Ω
Common Collector (No Phase Reversal)	Unity Gain	High Cutoff Frequency $\lesssim f_{\alpha b}$	Highest Input Resistance ~ 350 K Ω

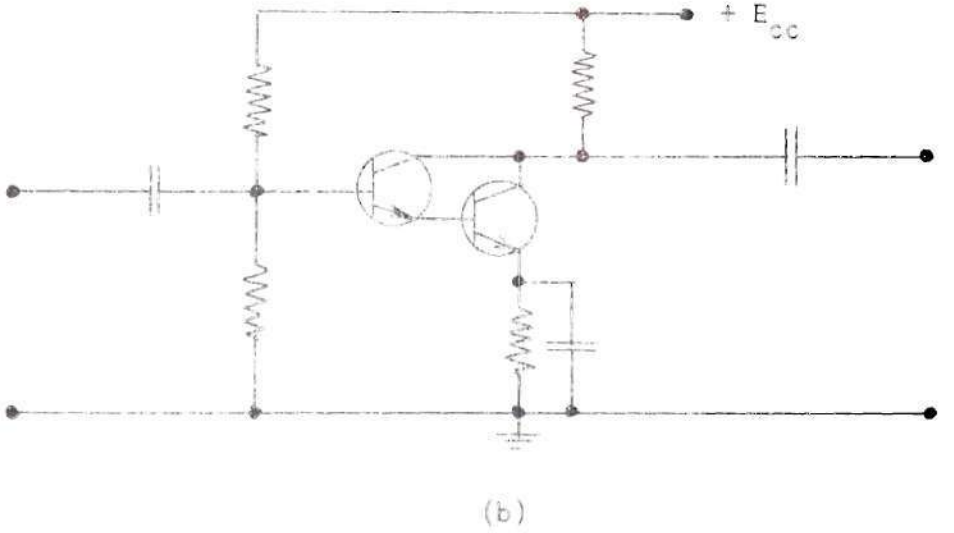
shown this to be too much gain to expect one stage to deliver. If two stages were to be used both would have to produce a fairly high gain and only one of the two could produce a phase reversal. Inspection of Table 1 shows that one stage would have to be common-emitter and one common-base. However, the low input impedance of a common-base stage would present difficulties. Therefore, a three stage amplifier was chosen.

Common-Emitter Common-Emitter Compound Connection

Since a single transistor in a common-emitter configuration has an inherently low input impedance it will be useful to consider a compound connection of two transistors. Figure 27a illustrates the C.E.C.E. compound



(a)



(b)

Figure 26. Possible Circuits for Second and Third Stages.

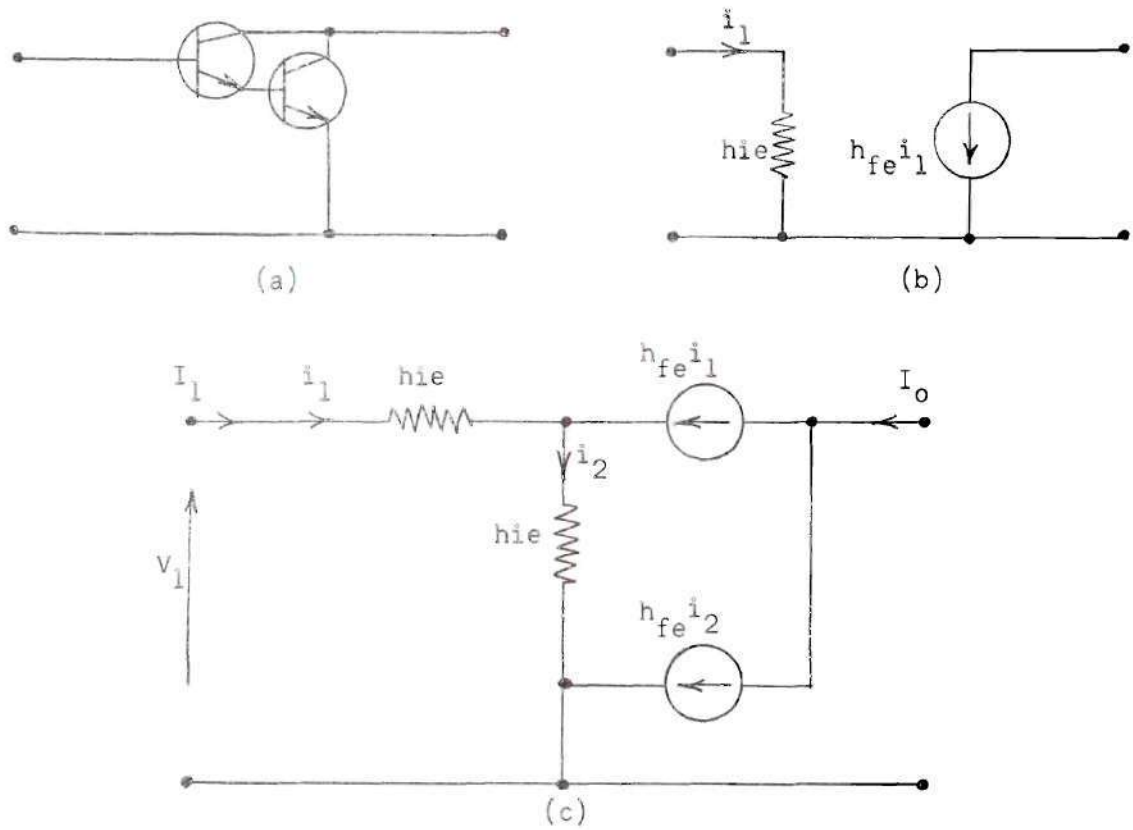


Figure 27. C.E.C.E. Compound Connection with Bypassed Emitter Resistor.

connection to be considered. Figure 27b is a hybrid model for a single transistor where the typically large collector-to-emitter resistance has been ignored. Figure 27c shows two hybrid models in the compound connection and with reference to Figure 27c it can be written that

$$i_2 = i_1 + h_{fe}i_1 = i_1(h_{fe} + 1)$$

$$V_1 = i_1 h_{ie} + i_2 h_{ie} = i_1 h_{ie} + i_1(h_{fe} + 1)h_{ie}$$

and since $I_1 = i_1$

$$V_1 = I_1(h_{fe} + 2)h_{ie}$$

or

$$h_{ie'} = \frac{V_1}{I_1} = (h_{fe} + 2)h_{ie} \tag{36}$$

Also, consider $h_{fe'}$ for the two transistors in compound. Referring again to Figure 27c it can be written that

$$h_{fe'} = \frac{I_o}{I_1}$$

where $I_o = h_{fe}i_1 + h_{fe}i_2 = h_{fe}(i_1 + i_2)$ and

$$i_2 = i_1(h_{fe} + 1)$$

so

$$I_o = i_1 h_{fe}(h_{fe} + 2)$$

and since $I_1 = i_1$

$$h_{fe'} = \frac{I_o}{I_1} = h_{fe}(h_{fe} + 2) \tag{37}$$

Now consider the C.E.C.E. compound connection with an unbypassed emitter resistor. For this case it can be written from Figure 28b that

$$h_{ie'} = \frac{V_1}{I_1}$$

where $V_1 = i_1 h_{ie} + i_2 h_{ie} + i_2(h_{fe} + 1) R_E$ and

$$i_2 = i_1(h_{fe} + 1)$$

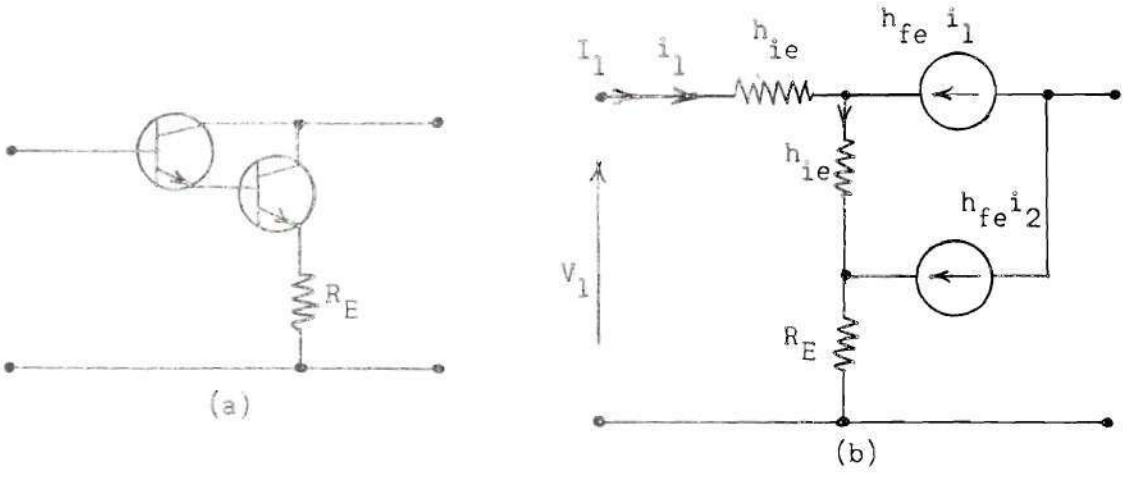


Figure 28. C.E.C.E. Compound Connection with Unbypassed Emitter Resistor.

so

$$V_1 = i_1 h_{ie} + i_1(h_{fe} + 1)h_{ie} + i_1(h_{fe} + 1)^2 R_E$$

$$V_1 = i_1 \left[h_{ie}(\beta + 2) + (\beta + 1)^2 R_E\right]$$

and since $I_1 = i_1$

$$h_{ie'} = \frac{V_1}{I_1} = h_{ie}\,(h_{fe} + 2) + R_E(h_{fe} + 2)^2 \qquad (38)$$

$h_{fe'}$ will, of course, still be given by Equation (37).

Selection of Transistors

The transistors most appropriate for the proposed problem can best be determined by first considering the requirements on them. The main requirements are listed as follows:

(a) A high cutoff frequency is desired so that a wideband amplifier can be constructed. This is to enable achievement of the stability requirements.

(b) A large β is desired so that high voltage gain and high input impedance can be obtained.

(c) A moderate-to-low noise figure is desired. This is especially important for the first amplifying stage.

(d) Stability with temperature changes is desired so that the overall circuit can be operated in a wide range of ambient temperatures.

Condition (d) immediately suggests the sole use of silicon transistors as opposed to germanium. This is because the leakage current in silicon units is less sensitive to changes in temperature than the leakage current in germanium units. Conditions (a) and (b) can be met by use of small signal mesa transistors. The alpha cutoff cutoff frequency (i.e. cutoff frequency for the transistor in common-base configuration) for a typical mesa transistor is

$$f_{\alpha b} = 250 \text{ mc/s}$$

For the common-emitter configuration the beta cutoff frequency is

$$f_{\alpha e} \simeq \frac{f_{\alpha b}}{h_{fe}} = \frac{250 \text{ mc/s}}{100} = 2.5 \text{ mc/s}$$

Here, the hybrid current amplification for the common-emitter configuration, h_{fe}, has been taken as 100. This is a typical value for h_{fe} for a mesa transistor. In lieu of using a special low noise transistor the mesa transistor will be assumed satisfactory for condition (c). A typical unit would have a moderate noise figure.

Although small signal transistors will be appropriate for the first two amplifier stages a medium power transistor may best meet the requirements

for the third stage. Recall that it is desired to have a large voltage swing on the dynamic operating path in the third stage. This is best achieved by using a medium power transistor since a larger voltage swing can be obtained without distortion than with a small signal device.

The Texas Instruments 2N736 n-p-n double-diffused silicon mesa transistor appears to be a satisfactory small signal device while the Texas Instruments 2N342 n-p-n grown junction silicon transistor appears to be an acceptable medium power unit. For the 2N736:

$$\text{Typical } h_{ie} \sim 1000\ \Omega$$

$$\text{Typical } h_{fe} \sim 100$$

From Equation (36), $h_{ie'}$ for the compound connection is approximately 100 KΩ even for a bypassed emitter resistor. Obviously, once the emitter resistor is omitted in the compound connection even higher input impedances can be achieved as seen by Equation (38). Now for the 2N342:

$$\text{Typical } h_{ie} \sim 1000\ \Omega$$

$$\text{Typical } h_{fe} \sim 35$$

Calculation of Parallel-T and Load Circuit Elements

Actual values for the elements in the load and parallel-T circuits will now be calculated using the procedure outlined in the latter part of Chapter II:

(a) Choose $K = .53$

(b) With reference to Figure 25a the parallel-T's output will be working into the impedance shown as Z_i in Figure 29. Using $h_{ie} \sim 1000\ \Omega$ and $h_{fe} \sim 100$ for the 2N736 in Equation (36), $h_{ie'} \sim 100$ KΩ. Choose $R = 100$ KΩ so that $R \| h_{ie'} \sim 50$ KΩ. $R_1 \| R_2$ will later be chosen to be

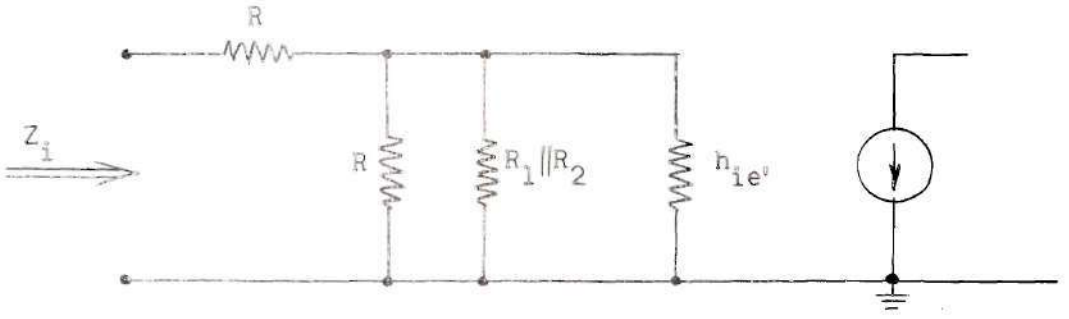


Figure 29. Circuit Showing Impedance Seen by Feedback Voltage.

much greater than 50 K Ω. So $Z_i \sim 150$ K Ω.

(c) Choose $1/G_o \ll Z_i$. Let $1/G_o = 5$ K Ω.

(d) Let $n = 1.0$. Now using Figure 15, $|Z_{11T} \| Z_{11L}|_{f_o} = 1770\ \Omega$. Also,

$$\frac{1}{G_o + G_1} = \frac{1}{G_o\left[1 + 2K\left(\frac{1+\sqrt{n+1}}{1+2\sqrt{n+1}}\right)\right]} \approx 3\ \text{K}\Omega$$

The d.c. load resistor on the last stage must be $\geq$ 3KΩ. Let this resistor be 3.1 KΩ and assume that the internal collector-to-emitter resistance (~80 K Ω) in parallel with this 3.1 KΩ results in about 3 KΩ on the input to the parallel-T.

(e) The d.c. load line and a dynamic operating path for the third stage are shown in Figure 31 for the circuit shown in Figure 30. A procedure for plotting the elliptical dynamic operating path is outlined

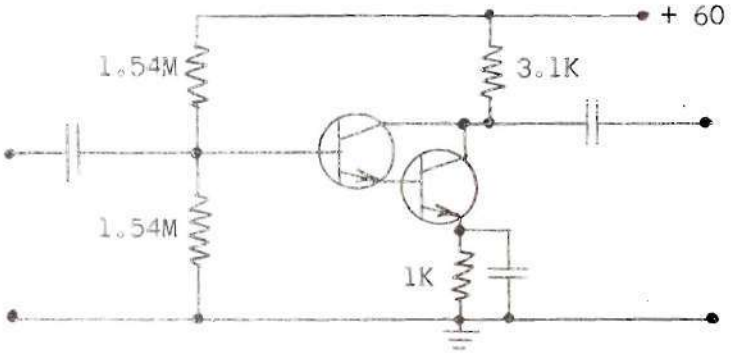


Figure 30. Final Amplifier Stage.

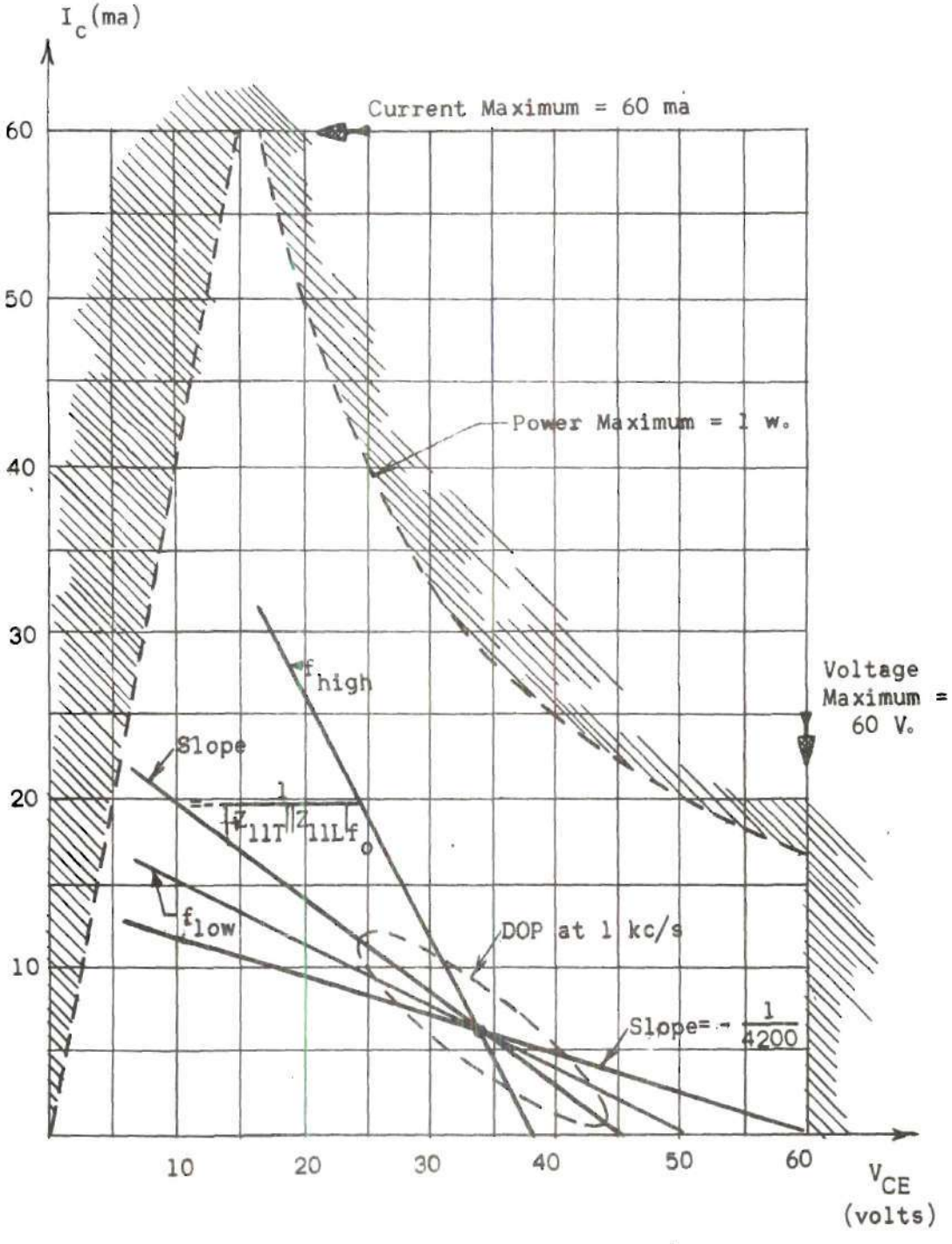


Figure 31. Allowed Operating Region for the T.I. 2N342 n-p-n Grown Junction Silicon Transistor at 25° C.

in the appendix. In Figure 31 the actual volt-ampere characteristics are not shown since they would have to be plotted for the compound connection and they are not that necessary. The dynamic operating path shown in Figure 31 is, of course, only for signal components at 1 kc/s. However, the major axes for high and low frequency D.O.P.'s are also shown. Preliminary experimentation has shown that some distortion will occur for the elliptical path as large as shown in Figure 31. Also, experimentation has shown that $|Z_{11T}||Z_{11L}|$ is not so large as to prevent this last stage from operating as a constant current source. By making the input signal somewhat smaller in magnitude to prevent distortion all requirements outlined in the latter part of Chapter II are met and the element values can now be calculated.

(f) From Equations (18), (19), (20), and (21) in Chapter II all parallel-T elements can be calculated. The results are:

$$\frac{1}{G_o} = 5\ K\Omega$$

$$C_a = C_b = .02247\ \mu f$$

$$\frac{1}{G_a} = \frac{1}{G_b} = 7.08\ K\Omega$$

Also, from Equations (30), (31), (32), (33), and (34) all load circuit elements can be calculated as: $C_1 = C_2 = .0222\ \mu f$, $\frac{1}{G_1} = 7.5\ K\Omega$, $\frac{1}{G_2} = 2.65\ K\Omega$ and $\frac{1}{G_3} = 5.06\ K\Omega$.

Voltage Gain Necessary for a Particular Q_{max}

With reference to Figure 32a it will prove useful to derive an equation for the amplifier's no-load voltage gain, V_2/V_1, as a function

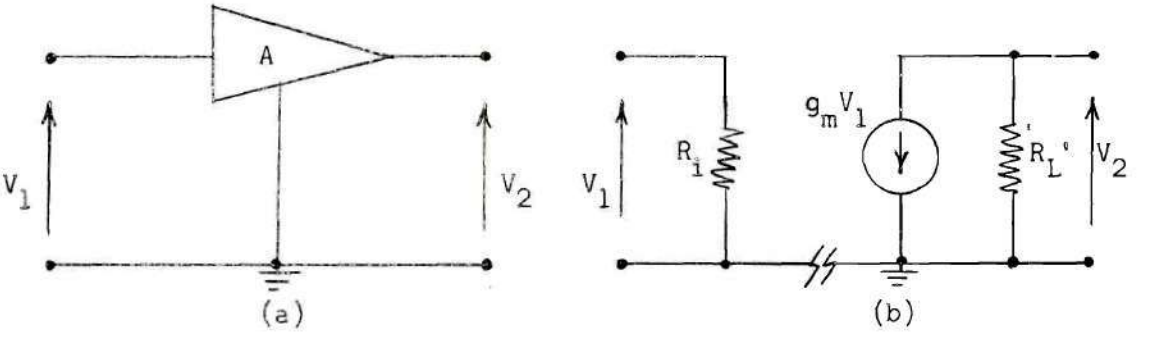


Figure 32. Overall Amplifier without Load.

of the Q_{max} desired in the overall circuit. In Figure 32b R_i represents the input resistance to the first stage and R_L' the a.c. load resistance on the last stage. Figure 33a will be assumed to be the type amplifier used for the last stage and Figure 33b is a valid hybrid model in the mid-frequency range where coupling and bypass capacitors are taken as short circuits. In Figure 33b R_X represents R_1 in parallel with R_2 and the load resistance on the preceding stage. R_L' in this figure represents R_L (see Figure 33a) in parallel with the internal collector-to-emitter resistance which is approximately 80 KΩ. Recall:

$$R_L = 3.1 \text{ K}\Omega$$

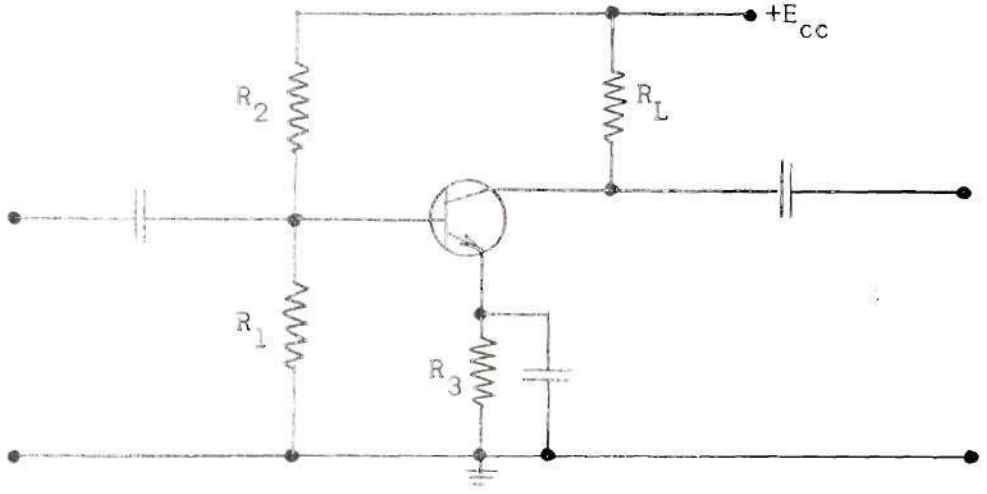
$$R_L' \approx 3 \text{ K}\Omega$$

With reference to Figure 32b write

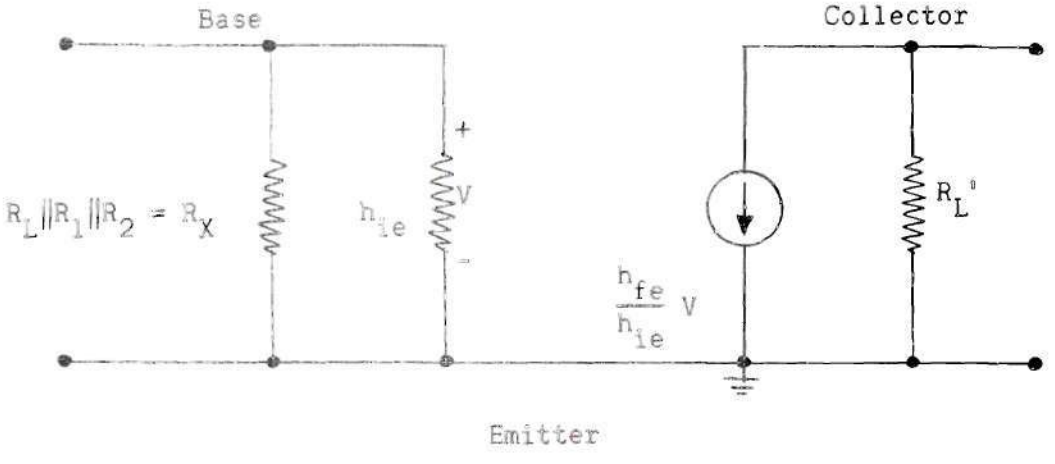
$$V_2 = -g_m V_1 R_L'$$

or

$$\frac{V_2}{V_1} = -g_m R_L'$$



(a)



(b)

Figure 33. Possible Configuration for Final Amplifying Stage.

Now write $Q_{max} = Q_o(1 + K_o)$ as

$$K_o = \frac{Q_{max} - Q_o}{Q_o}$$

and recall from Equation (7) that

$$K_o = \frac{g_m k}{2} \left(\frac{1}{G_o + G_a + G_b} \right)$$

or

$$K_o = \frac{g_m}{2(K + 1)\, G_o (1 + \sqrt{n+1})}$$

Equating the two equations for K_o there results

$$\frac{g_m}{2(K+1)\, G_o (1 + \sqrt{n+1})} = \frac{Q_{max} - Q_o}{Q_o}$$

or

$$g_m = \frac{2(K+1)\, G_o (1 + \sqrt{n+1})}{Q_o} (Q_{max} - Q_o)$$

Now for:

$$n = 1$$

$$K = .53$$

$$\frac{1}{G_o} = 5\ K\Omega$$

$$Q_o = \frac{\sqrt{n(n+1)}}{2(n+1)} = .354$$

and

$$g_m = (4.17 \times 10^{-3})\ (Q_{max} - .354) \qquad (39)$$

Now $V_2/V_1 = -g_m R_L' = -12.5(Q_{max} - .354)$ where R_L' is taken as 3 KΩ. Since any Q_{max} of interest will be much greater than .354 write

$$\frac{V_2}{V_1} \cong 12.5\, Q_{max} \tag{40}$$

From Equation (40) it can be seen that for $Q_{max} \sim 500$ the unloaded amplifier must have a voltage gain of 6,250.

Also, it will be useful to have a relationship between the overall voltage gain, K_e, for the proposed circuit at resonance and Q_{max}. Recall that

$$K_e = -(1-k)\, g_m \left(\frac{G_2}{C_2(G_1 + G_2)} \right) \frac{Q_o}{\omega_o}$$

Using $f_o = 1$ kc/s, $n = 1$, $K = \frac{1-k}{k} = .53$ and the circuit elements as previously calculated

$$K_e = -(6.5 \times 10^2)\, g_m$$

Using g_m from Equation (39) there results

$$K_e = -2.71\, (Q_{max} - .354)$$

or

$$K_e \cong -2.71\, Q_{max} \tag{41}$$

From Equation (41) it can be seen that for $Q_{max} \sim 500$ the overall circuit will have a voltage gain of 1,355 at $f = 1$ kc/s.

Additional Phase Shifts and Methods for Correction

A prime contributor to the closed loop phase shift will be the

series resistor in the feedback arm. Figure 34a shows the circuit to be used for the input summing stage and Figure 34b shows a hybrid model for this stage where coupling and bypass capacitors are taken as short circuits. It will now be necessary to include the internal base-to-emitter capacitance since it is also responsible for the phase shift. With reference to Figure 34b it can be written that

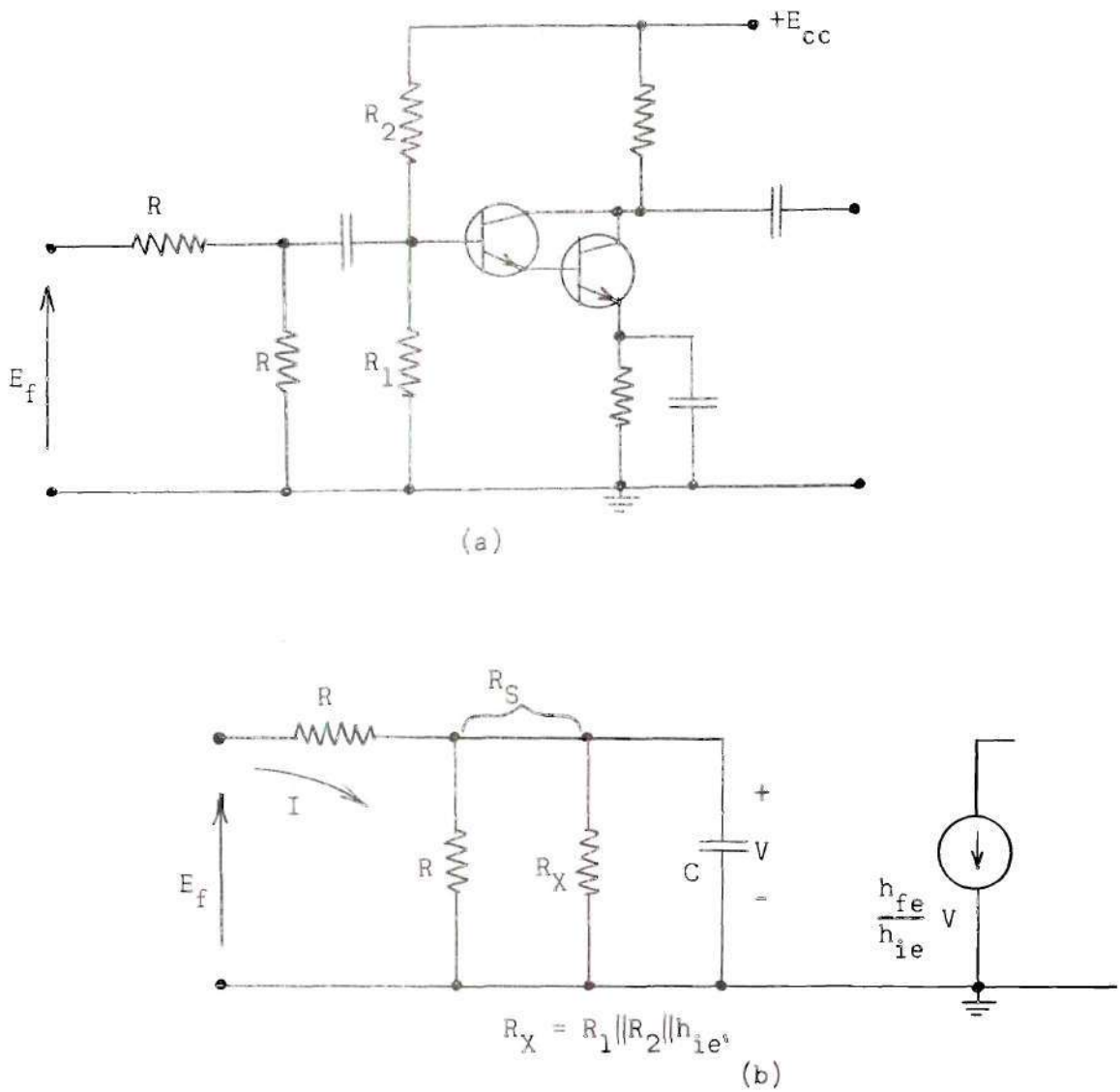


Figure 34. Circuits for Analysis of Phase Shift Associated with Series Feedback Resistor.

$$I = \frac{E_f}{R + \dfrac{1}{\dfrac{1}{R_S} + SC}} = \frac{E_f(1 + SR_SC)}{(R + R_S) + S(RR_SC)}$$

$$V = I\left(\frac{1}{\dfrac{1}{R_S} + SC}\right) = I\left(\frac{R_S}{1 + SR_SC}\right)$$

$$= \frac{E_f R_S}{(R + R_S) + j(\omega RR_SC)}$$

$$\frac{V}{E_S} = \left|\frac{V}{E_S}\right| \angle\varphi$$

where

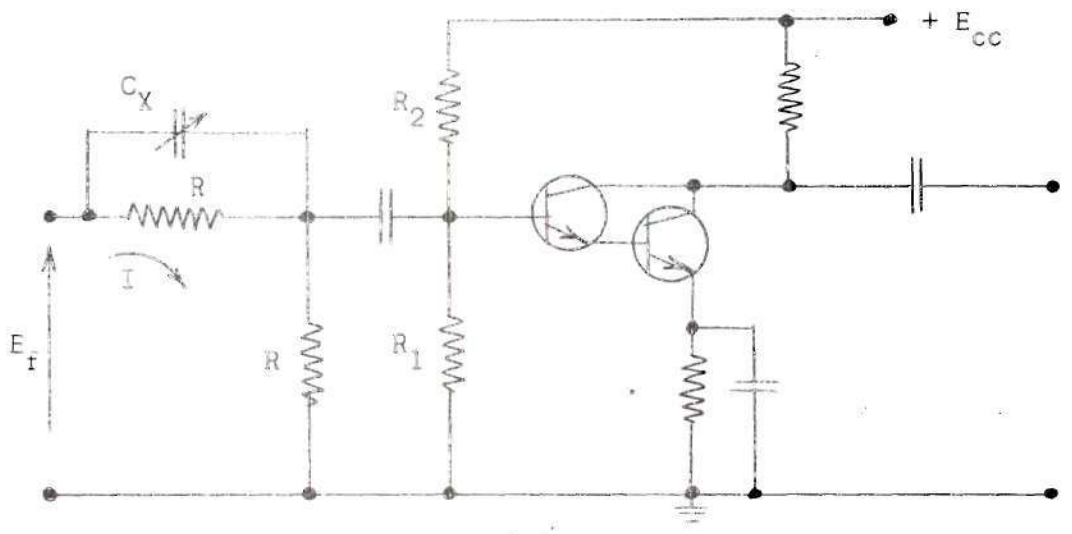
$$\varphi = -\operatorname{Tan}^{-1}\left(\frac{\omega RR_SC}{R + R_S}\right)$$

This will be a lagging phase shift and will approach $-90°$ as ω becomes very large. Fortunately this phase lag can be all but eliminated by placing a capacitor C_X in parallel with the series feedback resistor R as shown in Figure 35a. With reference to Figure 35b it can be written that

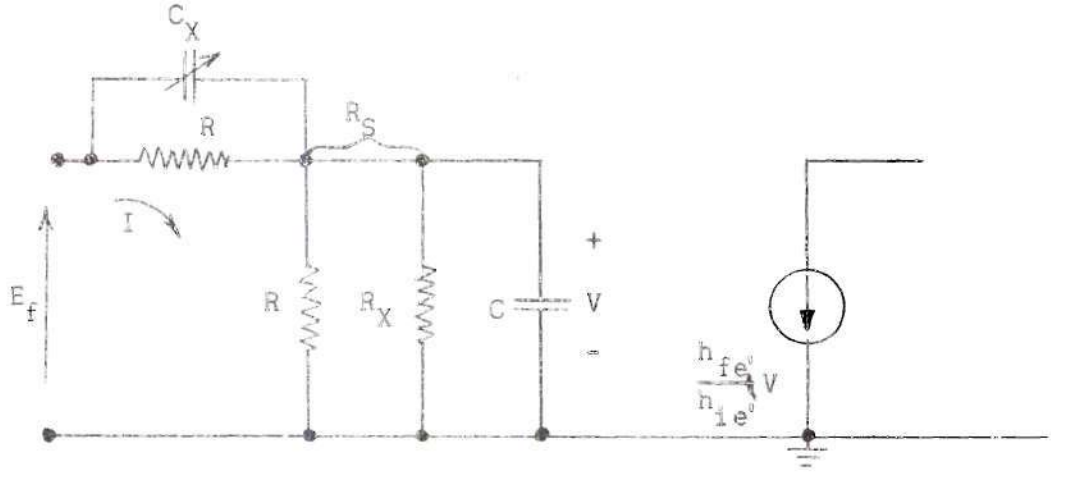
$$I = \frac{E_f}{\dfrac{1}{\dfrac{1}{R} + SC_X} + \dfrac{1}{\dfrac{1}{R_S} + SC}} = \frac{E_f}{\dfrac{R}{1 + SRC_X} + \dfrac{R_S}{1 + SR_SC}}$$

$$V = I\left(\frac{R_S}{1 + SR_SC}\right) = \frac{E_f R_S}{R\left(\dfrac{1 + SR_SC}{1 + SRC_X}\right) + R_S}$$

Now if C_X is chosen so that $RC_X = R_SC$



(a)



$R_X = R_1 \| R_2 \| h_{ie'}$

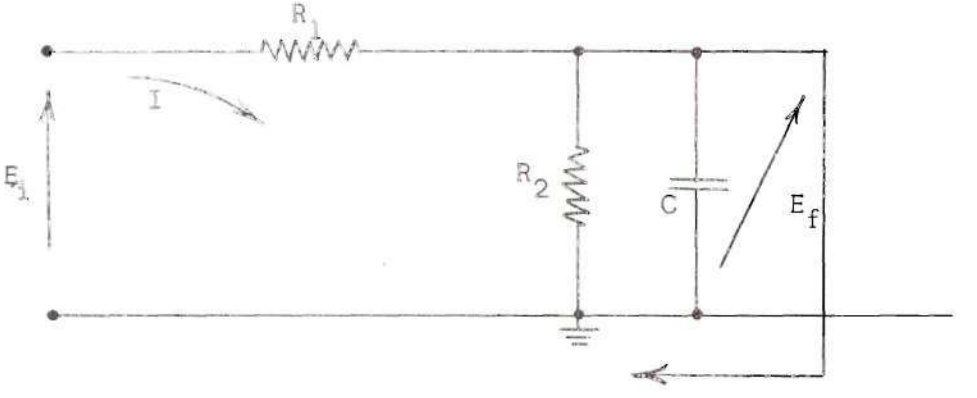
(b)

Figure 35. Phase Correction Technique.

$$\frac{V}{E_f} = \frac{R_S}{R + R_S} \quad \angle 0°$$

A satisfactory method for determining C_X is to use a small variable capacitor and to vary if for stable operation of the overall circuit. The procedure will be to set the input signal at f_o = 1 kc/s and gradually increase β from zero until instability results. At this point vary C_X slightly until the output again appears stable. Now again increase β and correct with C_X. In the experimental circuit C_X was simply two short pieces of insulated wire braided together. C_X was varied by clipping off wire.

The resistor on the output of the parallel-T network, $1/G_o$, will also produce a sizeable phase shift.



$$R_1 + R_2 = 1/G_o$$

C = Parasitic Capacitance Between the Feedback Arm and Ground

Figure 36. Circuit for Analysis of Phase Shift Associated with Parallel-T Output Resistor.

From Figure 36

$$I = \frac{E_i}{R_1 + \dfrac{1}{\dfrac{1}{R_2} + SC}} = \frac{E_i(1 + SR_2C)}{(R_1 + R_2) + S(R_1R_2C)}$$

$$E_f = I\left(\frac{1}{\dfrac{1}{R_2} + SC}\right) = I\left(\frac{R_2}{1 + SR_2C}\right)$$

$$= \frac{E_iR_2}{(R_1 + R_2) + j(\omega R_1R_2C)}$$

$$\frac{E_f}{E_i} = \left|\frac{E_f}{E_i}\right| \angle\varphi, \text{ where } \varphi = -\text{Tan}^{-1}\left(\frac{\omega R_1R_2C}{R_1 + R_2}\right)$$

One way to eliminate this phase shift would be to place a variable capacitor C_1 in parallel with R_1 and vary it in such a way that $R_1C_1 = R_2C$ as β goes from zero to unity. This would eliminate phase shift for all values of β but would be difficult to achieve physically. Another possibility would be to place a fixed capacitor C_1 in parallel with R_1 so that $R_1C_1 = R_2C$ where the phase shift is a maximum. Now it must be determined where the phase shift is a maximum.

$$\varphi = -\text{Tan}^{-1}\left(\frac{\omega R_1R_2C}{R_1 + R_2}\right)$$

Recall that $R_1 + R_2 = \frac{1}{G_o}$. Now

$$R_2 = \beta\left(\frac{1}{G_o}\right)$$

and

$$R_1 = \frac{1}{G_o} - R_2 = \frac{1}{G_o}(1 - \beta)$$

so

$$\varphi = -\operatorname{Tan}^{-1}\left(\frac{\omega C \left(\frac{1}{G_o}\right)^2 (1 - \beta)\beta}{\frac{1}{G_o}}\right)$$

$$= -\operatorname{Tan}^{-1}\left(\omega C \left(\frac{1}{G_o}\right) (1 - \beta)\beta\right) \qquad (42)$$

To determine the value of β for φ_{max} set

$$\frac{d(1 - \beta)\beta}{d\beta} = 0$$

From this it can be shown that $\beta = .5$ corresponds to φ_{max}. Therefore, by making $C_1 = C$ the maximum phase shift that originally occurred can be eliminated. However, phase shift will still occur as β is varied from 0 to .5 and from .5 to 1.0, but to a lesser degree. The actual value of C_1 to be used is best determined under actual operating conditions and will be that value which produces the most stable output. Figure 37 shows C_1 on the output of the parallel-T. Also, from Equation (42) it can be seen that the smaller the value for $1/G_o$ the less the phase shift

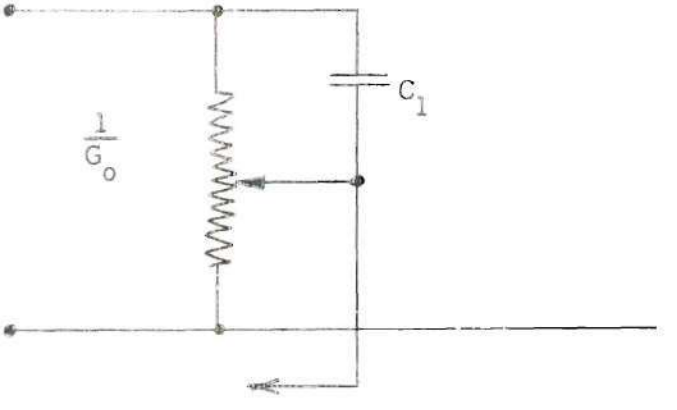


Figure 37. Phase Correction Technique.

Also, there will be a phase shift associated with the parallel-T's transfer impedance as shown in Figure 12. This is a leading phase shift for $f > 1$ kc/s and lagging for $f < 1$ kc/s. Therefore, this phase shift will not contribute to instability because it always opposes the phase shift introduced by the amplifier's cutoff. In fact, the parallel-T phase shift will contribute slightly to stability.

Experimental Circuit

Figure 38 shows the circuit constructed to meet all criteria previously discussed. The parallel-T network was tuned to 1 kc/s by the procedure outlined in the appendix. Note that the three stages comprising the amplifier have the same configurations as proposed earlier in this chapter. The variable capacitors shown across the series feedback resistor and across the output potentiometer in the parallel-T were selected for the most stable output at E_2. Of these two capacitors the one across the feedback resistor has the greater effect on the overall stability and care was taken to choose the best value. For this circuit: $|E_2/E_1|_{f_o} \sim 1350$ resulting in a predicted Q_{max} from Equation (41) of

$$Q_{max} \sim \frac{1350}{2.71} \sim 500$$

The circuit constructed has several disadvantages which are considered as follows:

(a) The response of the amplifier section is not wide enough for correct operation when $\beta \cong 0$ or $Q_{overall} \sim Q_o$.

(b) Noise is apparent in the final output, E_2, for $\beta \cong 0$. However, this noise rapidly disappears as β is increased from zero.

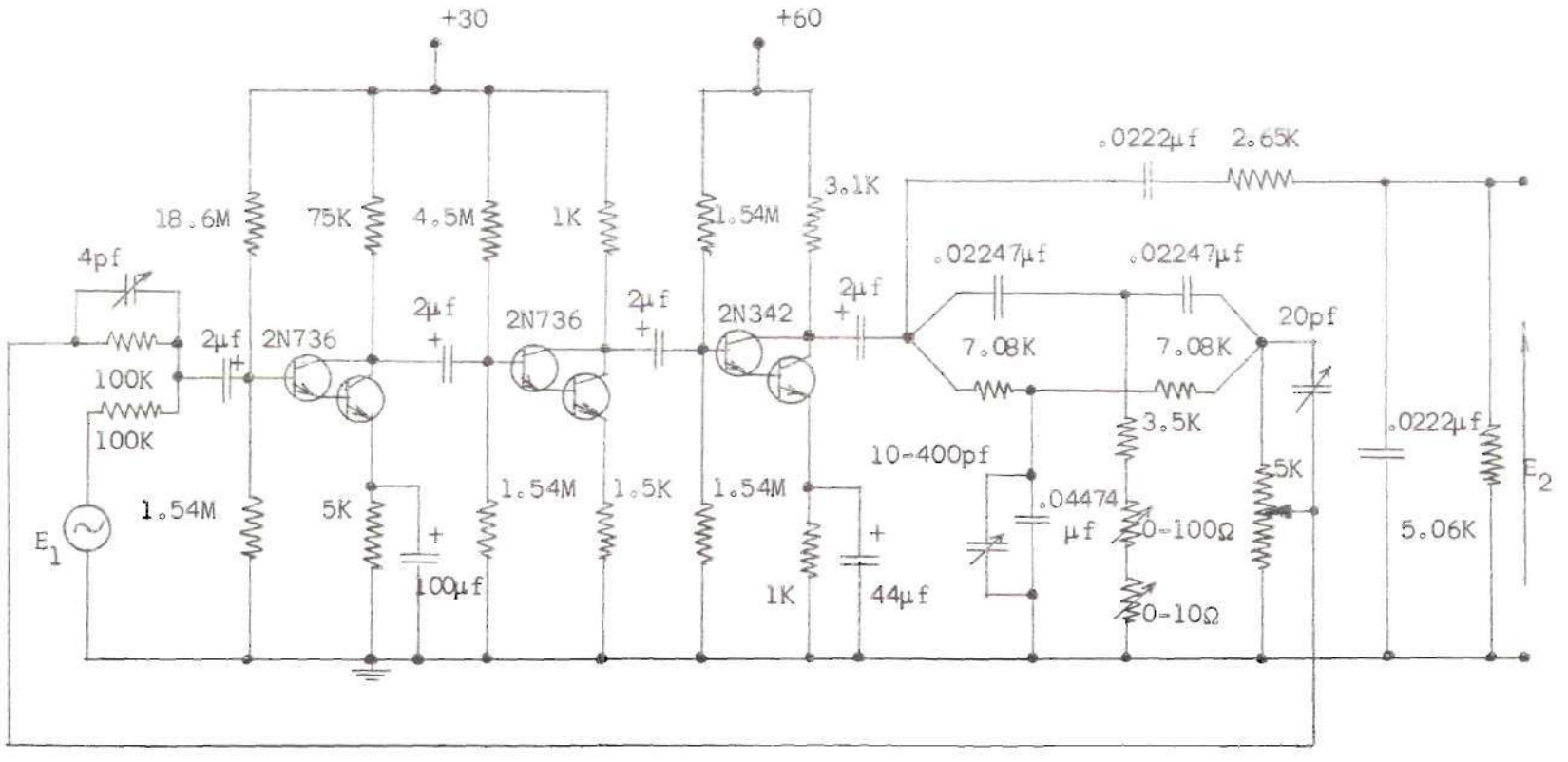


Figure 38. Experimental Circuit.

(c) The operating Q-points tend to shift slightly as the three stages are coupled together. This is believed to be caused by parasitic coupling between stages. For example, in one instance the presence of a nearby d.c. voltmeter caused a Q-point to shift from $V_{CE} \sim 20$ volts to $V_{CE} \sim 50$ volts even though the meter was not connected directly to the circuit. In this instance the removal of the meter eliminated the problem, but all experimentation was plagued by similar problems. On occasion the shift in Q-point was sufficient to result in destruction of the transistors involved.

(d) Traces of 60 c/s pickup are apparent in the output.

Because of items (c) and (d) above, care was taken to shield the entire circuit. Each amplifier stage was enclosed in an aluminum box as were the load and feedback circuits. Also, all leads from the oscillator, d.c. supply, oscilloscope and the V.T.V.M. were made of shielded cable. The purpose was to reduce parasitic capacitive coupling and to prevent a shift in Q-points. The result was that the Q-points were made more stable upon coupling of stages although they still shifted slightly. Since iron or soft steel is required for 60 c/s shielding the above procedure was not expected to reduce the 60 c/s appreciably. However, the use of copper shielded cables did appear to reduce the 60 c/s pickup somewhat. Also, a portion of the internal circuit wiring was done with shielded cable. In particular, the lead used for the feedback from the parallel-T to the input stage was shielded.

CHAPTER IV

MEASUREMENTS

Instrumentation

Measurements were made on the circuit of Figure 38 to gain insight into its operation. Several pieces of equipment were required for this and the following were used:

a. Tektronix oscilloscope Type 514 AD

b. Hewlett Packard oscilloscope Model 120 A

c. Electronic Research Associates Inc. tubeless power supply Model 110 DMC

d. Hewlett Packard oscillator Model 200 CD

e. Hewlett Packard vacuum tube voltmeter Model 400 D

f. General Radio wave analyzer Type 736 A

The Hewlett Packard oscilloscope was used to make phase shift measurements. A clear plastic mask was placed on the screen to read phase shifts directly without any calculations necessary. The wave analyzer was used in tuning the parallel-T network to 1 kc/s.

Amplifier Response

The amplitude and phase responses will first be considered for the three individual stages and then the responses for the unloaded three stage amplifier will be considered.

Table 2 gives pertinent data for the three stages taken individually. Using the high and low cutoff frequencies as given in Table 2 an asymptotic

Table 2. Data for Individual Transistor Stages

	Q-Point		Mid-Band Gain (db)	High Cutoff Frequency (kc/s)	Low Cutoff Frequency (kc/s)	Input Resistance R_i (K Ω)
	V_{CE} (volts)	I_C (ma)				
Stage 1	15	.187	38.80	3.75	~ 0	165
Stage 2	21	3.15	-5.32	700	~ 0	700
Stage 3	34	6.34	44.30	42	.23	4.98

amplitude response is plotted in Figure 39. Note that the individual responses are such that the composite three stages should produce a response symmetrical about f_o = 1 kc/s. All measurements on the first stage were made with the feedback input at ground potential. The phase shift for each stage can be predicted by using the cutoff frequencies as given and the rules governing asymptotic phase shifts. Figure 40 shows the phase shift for each individual stage and the sum of these individual phase shifts is also shown. The input resistance for each stage was measured by placing a resistor in series with the amplifier's input, such as R in Figure 41, and measuring the voltages V_1 and V_2 with the V.T.V.M. With reference to Figure 41 the input resistance R_i is given by

$$R_i = \frac{V_1}{I_1} - R$$

where

$$I_1 = \frac{V_1 - V_2}{R}$$

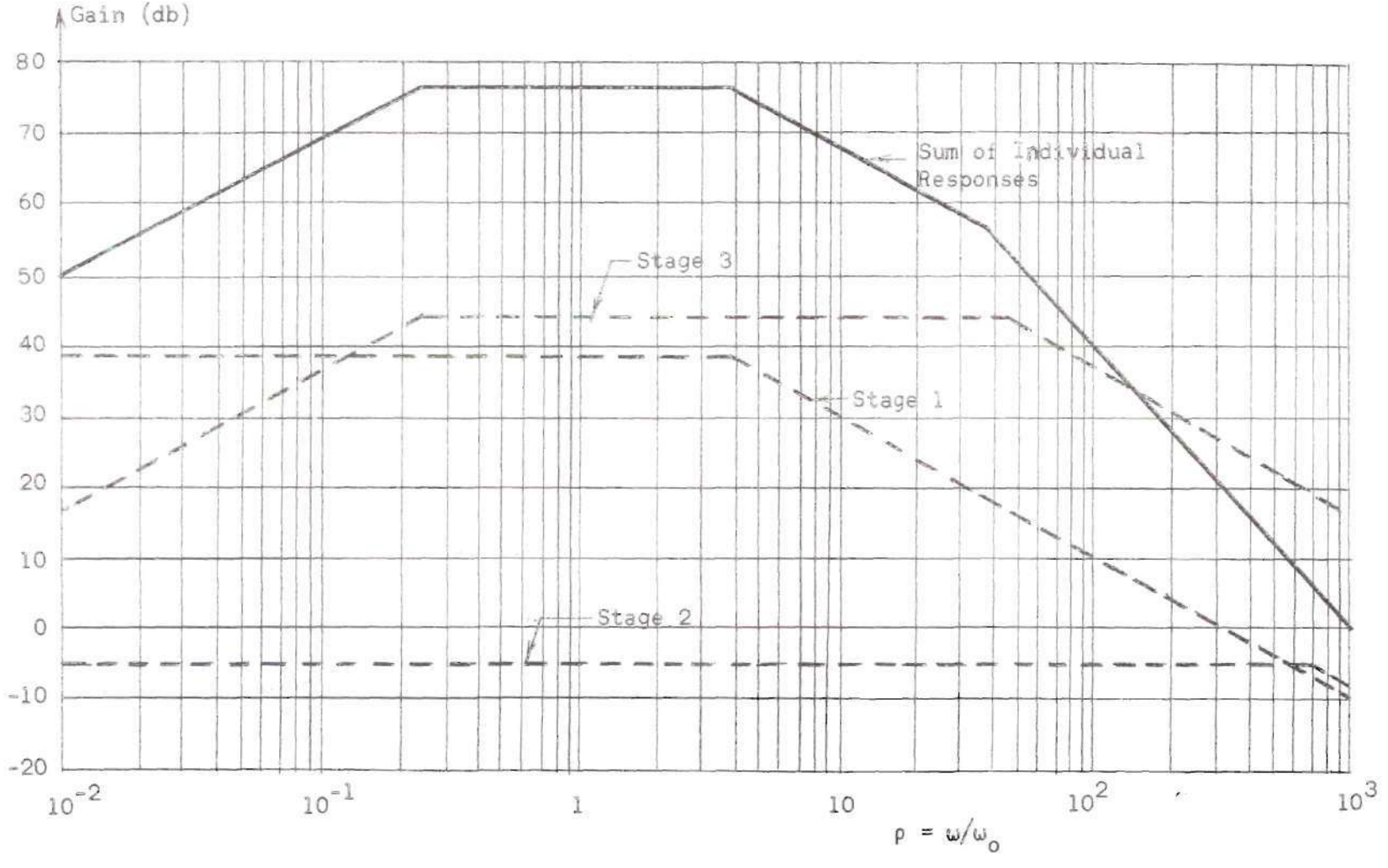


Figure 39. Asymptotic Amplitude Responses for Individual Stages.

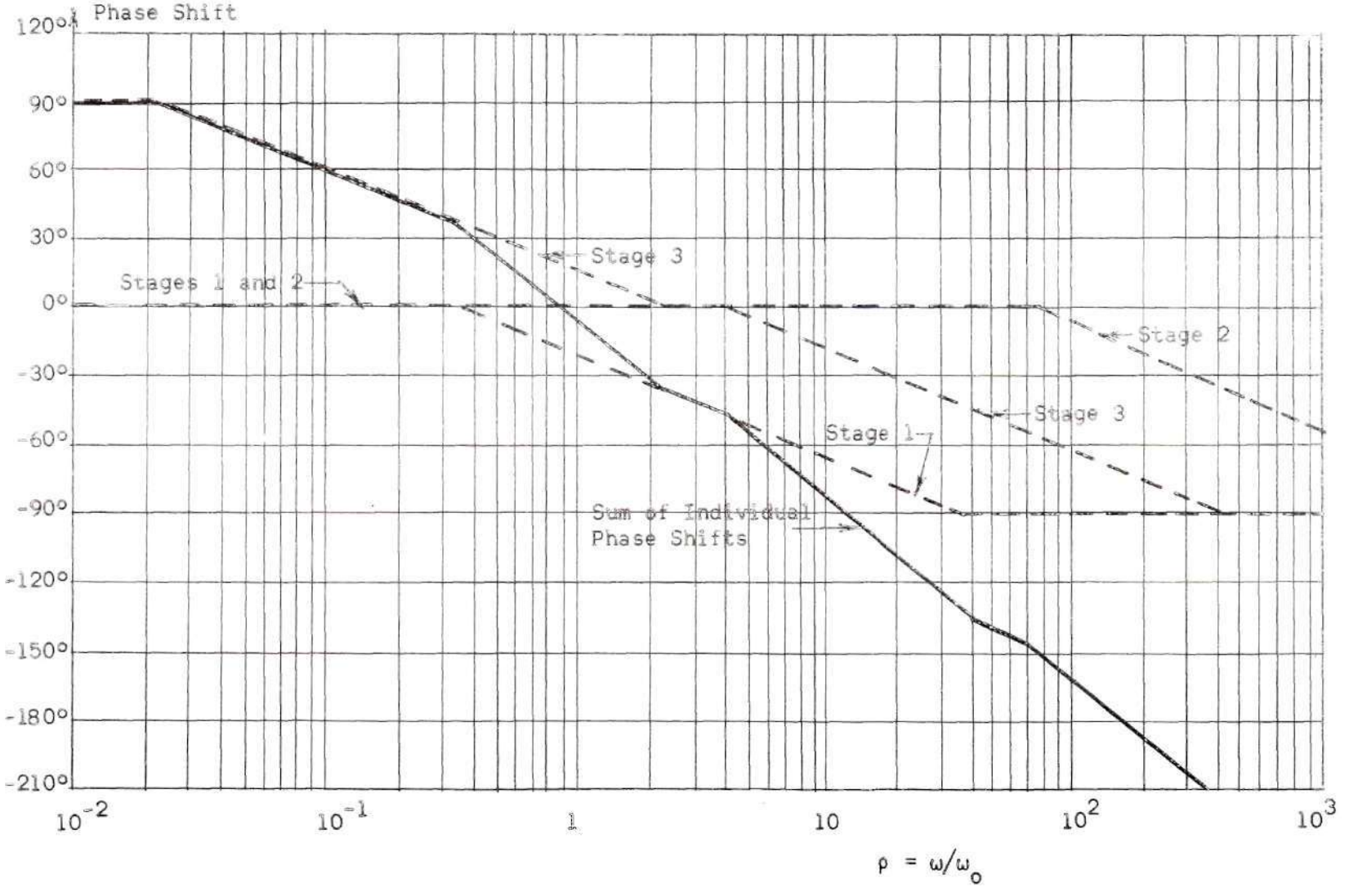


Figure 40. Asymptotic Phase Shifts for Individual Stages

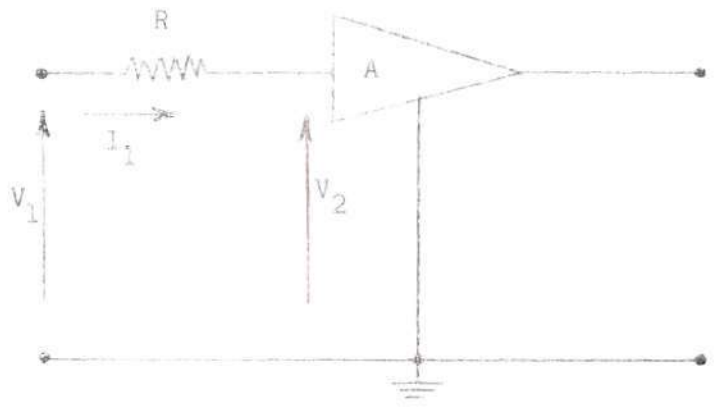


Figure 41. Circuit Used to Measure Input Resistance R_i.

so

$$R_i = \left(\frac{V_1}{V_1 - V_2}\right) R - R = R \left(\frac{V_2}{V_1 - V_2}\right)$$

Table 3 gives data for the voltage gain in the unloaded three stage amplifier. This data is plotted in Figure 42 along with the predicted amplitude response from the individual stages. Note that the actual gain compares favorably with that predicted by the cutoff frequencies and gains for the individual stages. Table 4 gives the phase shift in the unloaded three stage amplifier. This is plotted in Figure 43 along with the predicted phase shift from the individual stages. The actual phase shift is similar to that predicted.

Recall Equation (40) which is restated as

$$\left|\frac{V_2}{V_1}\right|_{f_o} \cong 12.5\, Q_{max}$$

where V_2/V_1 is the voltage gain for the unloaded three stage amplifier. From Table 3 this gain is 76 db or 5,320 at f_o = 1 kc/s. Therefore,

Table 3. Voltage Gain for Unloaded Three Stage Amplifier

Frequency	Voltage Gain (db)
10 c/s	52.3
30 c/s	60.9
60 c/s	66.5
100 c/s	70.2
200 c/s	73.5
400 c/s	75.5
700 c/s	76.0
1 kc/s	76.0
2 kc/s	75.6
4 kc/s	74.2
8 kc/s	71.1
10 kc/s	69.5
20 kc/s	63.3
40 kc/s	54.6
80 kc/s	45.0
100 kc/s	42.5
200 kc/s	39.3
400 kc/s	37.3
600 kc/s	35.5

$$Q_{max} \cong \frac{6320}{12.5} = 506$$

Parallel-T Response

Measurements on the parallel-T's amplitude and phase responses were made with the parallel-T operating in the overall circuit for $\beta = 0$. (i.e. no feedback). Figure 44 shows the circuit as it was used for measurements on the parallel-T.

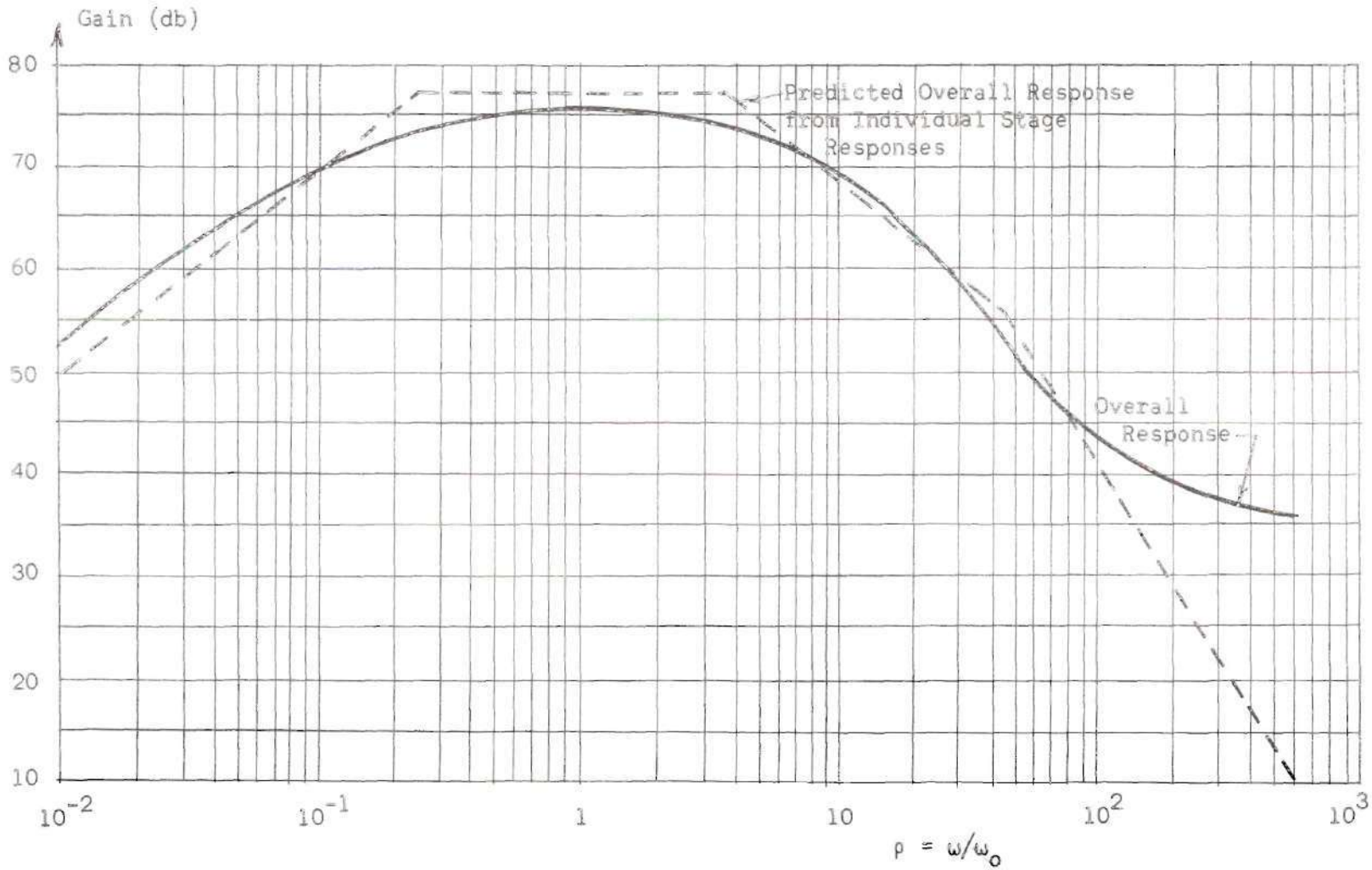


Figure 42. Voltage Gain for Unloaded Three Stage Amplifier.

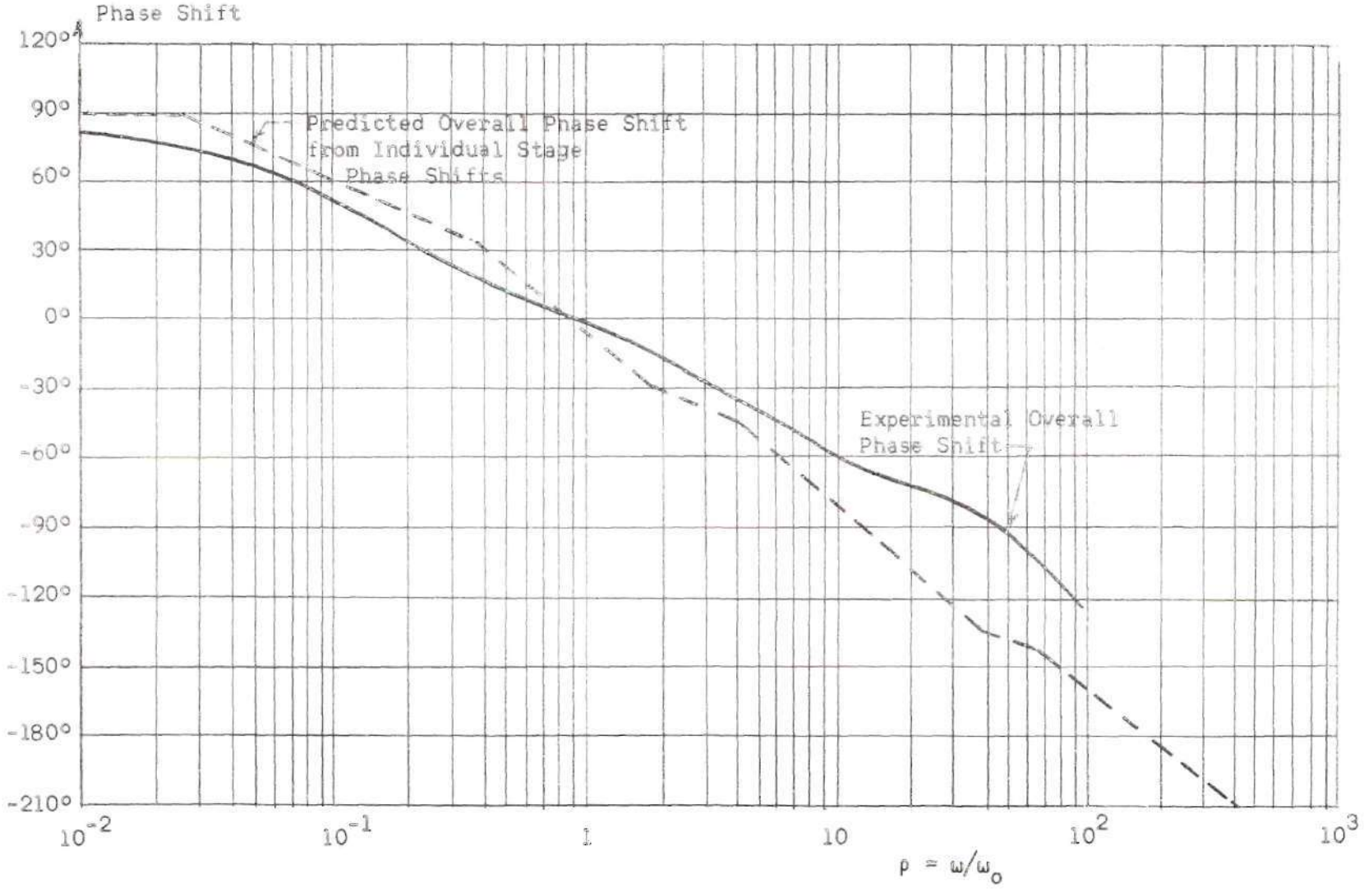


Figure 43. Phase Shift Through Unloaded Three Stage Amplifier.

Table 4. Phase Shift for Unloaded Three Stage Amplifier

Frequency	Phase Shift (Degrees)
10 c/s	+ 85
20 c/s	+ 80
60 c/s	+ 70
100 c/s	+ 60
200 c/s	+ 38
300 c/s	+ 25
400 c/s	+ 20
500 c/s	+ 15
800 c/s	+ 5
1.0 kc/s	0
1.2 kc/s	- 5
1.5 kc/s	- 10
2.0 kc/s	- 15
3.0 kc/s	- 28
4.0 kc/s	- 35
8.0 kc/s	- 50
10.0 kc/s	- 58
15.0 kc/s	- 64
20.0 kc/s	- 68
30.0 kc/s	- 75
40.0 kc/s	- 80
60.0 kc/s	- 105
100.0 kc/s	- 120

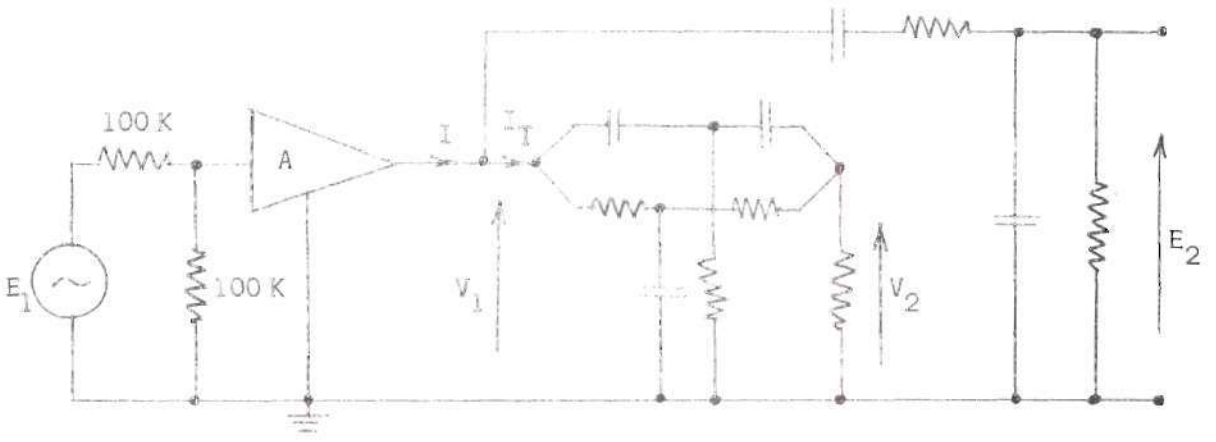


Figure 44. Circuit Used for Measurements on Parallel-T.

With reference to Figure 44, voltages V_1 and V_2 were measured with the Hewlett Packard V.T.V.M. However, it is desirable to also determine I_T so that $|V_2/I_T|$ can be plotted and compared with the transfer impedance of Figure 11 in Chapter II. Obviously

$$I = \frac{V_1}{|Z_{11T} \| Z_{11L}|}$$

and recalling that $I_T = I\left(\frac{1}{K+1}\right) = I\left(\frac{1}{1.53}\right) = .654\, I$ it can be written that

$$I_T = \frac{.654\, V_1}{|Z_{11T} \| Z_{11L}|}$$

$|Z_{11T} \| Z_{11L}|$ can be determined from Figure 15 in Chapter II. Table 5 contains all pertinent data arriving at $|V_2/I_T|$. Figure 45 is a plot of $|V_2/I_T|$ along with the theoretical transfer impedance from Figure 11 in Chapter II. With reference to Table 5 the attenuation at resonance is given in decibels by

Table 5. Transfer Impedance for Parallel-T

Frequency	V_1 (volts rms)	V_2 (volts rms)	$\lvert Z_{11T} \rVert Z_{11L} \rvert$ from Fig. 15 (ohms)	$I_T = \frac{.654\ V_1}{\lvert Z_{11T} \rVert Z_{11L} \rvert}$ (ma)	$\lvert V_2/I_T \rvert$ (ohms)
20 c/s	.60	.158	2600	.151	1048
60 c/s	1.75	.455	2585	.442	1030
100 c/s	2.63	.675	2550	.674	1000
200 c/s	3.75	.900	2415	1.017	885
400 c/s	4.20	.770	2190	1.250	616
500 c/s	4.30	.660	2095	1.340	492
600 c/s	4.20	.510	2020	1.360	375
700 c/s	4.10	.360	1945	1.378	261
800 c/s	4.00	.238	1880	1.390	171
900 c/s	3.90	.114	1830	1.393	82
1.0 kc/s	3.80	.052	1770	1.403	37
1.5 kc/s	3.30	.410	1578	1.368	300
2.0 kc/s	2.92	.655	1440	1.325	493
3.0 kc/s	2.27	.870	1225	1.210	718
4.0 kc/s	1.80	.920	1080	1.090	833
6.0 kc/s	1.23	.845	907	.888	951
8.0 kc/s	1.03	.820	817	.825	993
10.0 kc/s	.86	.717	776	.720	995
20.0 kc/s	.44	.415	710	.405	1028
40.0 kc/s	.23	.225	687	.219	1028
80.0 kc/s	.13	.125	680	.125	1000

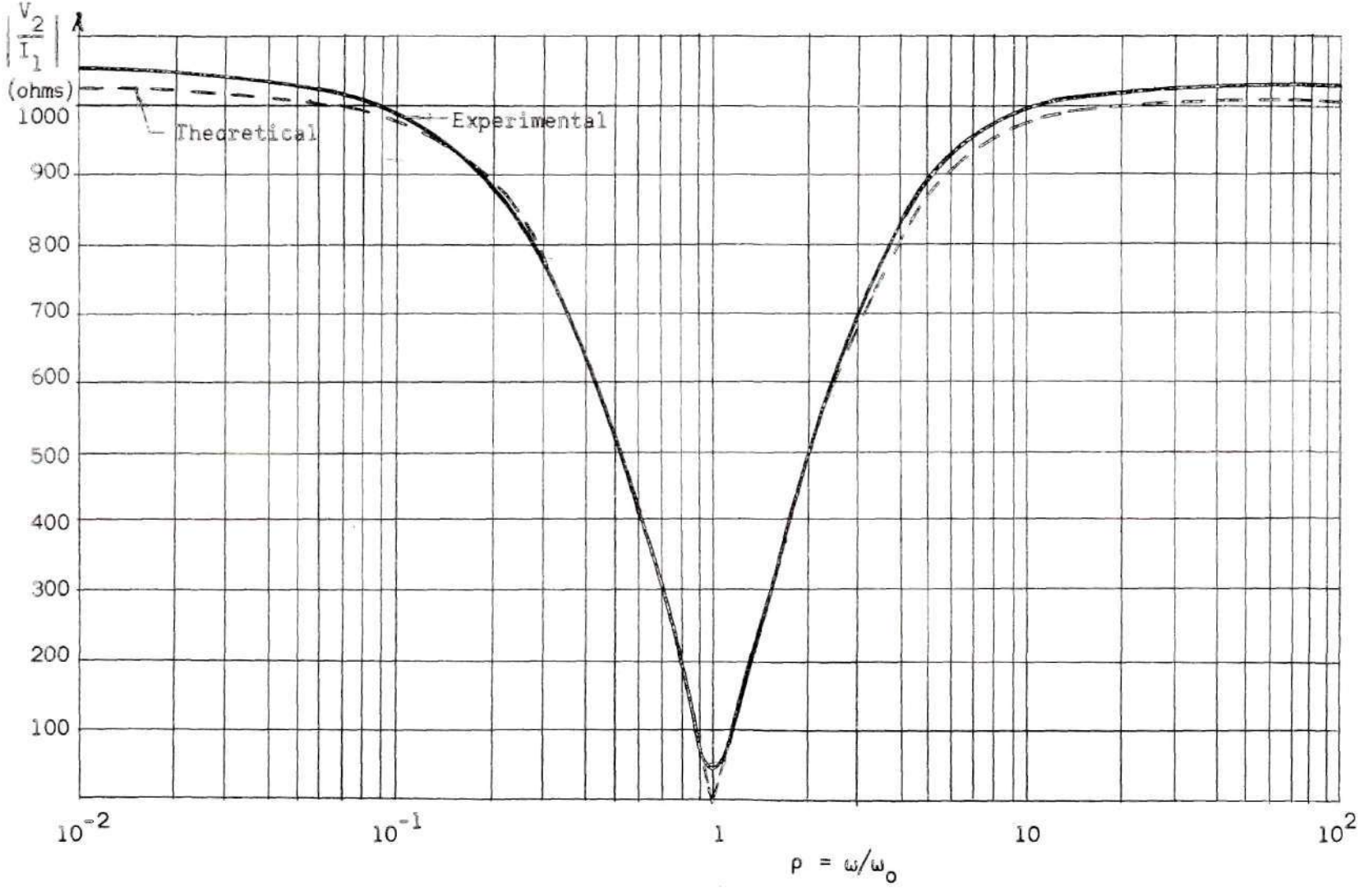


Figure 45. Parallel-T Transfer Impedance.

$$\text{Attenuation at } f_o \text{ in db} = 20 \log \frac{37}{1048} = -29 \text{ db}$$

However, this measurement may not give the true attenuation at resonance since it was made with a wideband V.T.V.M. and harmonics may have been present in V_2 at $f_o = 1$ kc/s. Table 6 contains data on the phase shift associated with V_2/V_1 from Figure 44. This data is plotted in Figure 46. A plot of the phase shift associated with V_2/I_1 would be similar to Figure 46.

Overall Response

The circuit of Figure 38 will now be used to make measurements on the overall response, E_2/E_1, for several values of β. Tables 7, 8, 9, 10, 11 and 12 contain the data collected for $\beta = 0$, .00129, .0048, .00804, .0269 and .128 respectively. The normalized frequency responses for these values of β are plotted in Figure 47. The dashed curve in Figure 47 shows what the $\beta = 0$ curve would look like if the amplifier section produced a flat response over the entire range from 10 c/s to 100 kc/s. Note that the voltage gain at $f_o = 1$ kc/s is always close to 1,360. Recalling Equation (41), which is restated here as

$$\left|\frac{E_2}{E_1}\right|_{f_o} \cong 2.71 \quad Q_{max} ,$$

Q_{max} is seen to be

$$Q_{max} \cong \frac{1,360}{2.71} = 503$$

However, the actual Q_{max} achieved can only be determined by considering the actual response for $\beta = 1$.

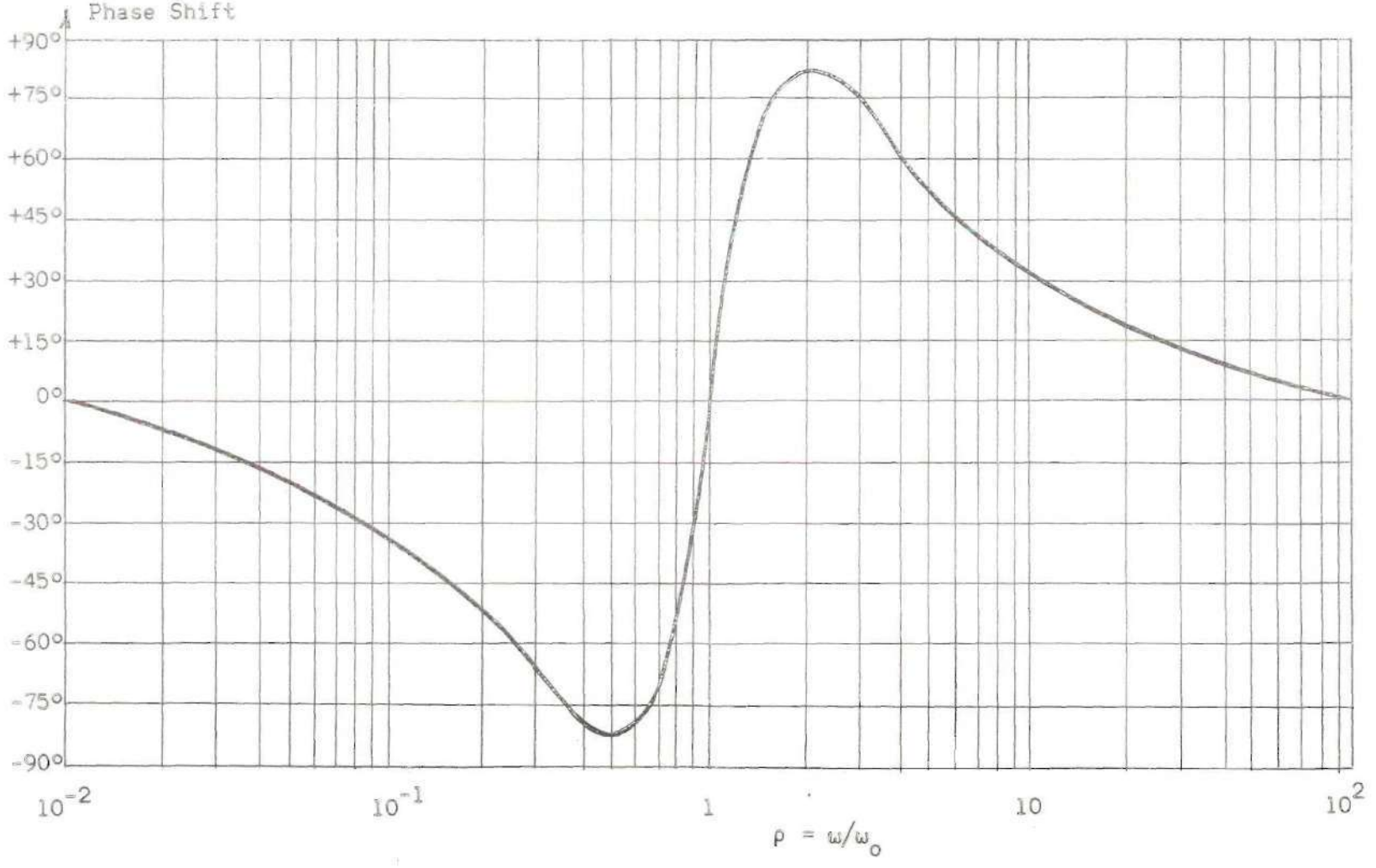


Figure 46. Phase Shift in Parallel-T.

Table 6. Phase Shift in Parallel-T Associated with V_2/V_1 in Figure 44

Frequency	Phase Shift (Degrees)
25 c/s	- 9°
50 c/s	-19°
80 c/s	-29°
100 c/s	-34°
200 c/s	-54°
300 c/s	-69°
500 c/s	-85°
600 c/s	-78°
700 c/s	-69°
800 c/s	-55°
900 c/s	-39°
1.0 kc/s	0°
1.2 kc/s	+50°
1.4 kc/s	+65°
1.5 kc/s	+70°
1.6 kc/s	+75°
1.8 kc/s	+80°
2.0 kc/s	+85°
3.0 kc/s	+75°
4.0 kc/s	+63°
6.0 kc/s	+50°
8.0 kc/s	+40°
10.0 kc/s	+33°
15.0 kc/s	+24°
20.0 kc/s	+20°
40.0 kc/s	+10°

Table 7. Overall Voltage Gain for $\beta = 0$

Frequency	$\lvert E_2/E_1 \rvert$	Normalized
20 c/s	16	.0114
60 c/s	75	.0550
100 c/s	187	.1375
200 c/s	522	.3840
400 c/s	1025	.7530
600 c/s	1250	.9200
800 c/s	1345	.9800
1.0 kc/s	1360	1.0000
1.5 kc/s	1274	.9375
2.0 kc/s	1147	.8430
4.0 kc/s	665	.4880
8.0 kc/s	252	.1850
10.0 kc/s	173	.1270
20.0 kc/s	47	.0348
40.0 kc/s	16	.0121
80.0 kc/s	13	.0095
100.0 kc/s	13	.0094

Table 8. Overall Voltage Gain for $\beta = .00129$

Frequency	$\lvert E_2/E_1 \rvert$	Normalized
20 c/s	13	.0091
60 c/s	61	.0445
100 c/s	125	.0923
200 c/s	301	.2210
300 c/s	460	.3380
400 c/s	645	.4730
800 c/s	1247	.9170
1.0 kc/s	1360	1.0000
1.2 kc/s	1267	.9300
1.5 kc/s	1066	.7830
2.0 kc/s	789	.5790
3.0 kc/s	510	.3750
4.0 kc/s	372	.2730
8.0 kc/s	166	.1220
10.0 kc/s	125	.0920
20.0 kc/s	42	.0311
40.0 kc/s	14	.0106

Table 9. Overall Voltage Gain for β = .0048

Frequency	$\lvert E_2/E_1 \rvert$	Normalized
20 c/s	10	.0073
60 c/s	39	.0288
100 c/s	71	.0520
200 c/s	149	.1100
300 c/s	236	.1740
400 c/s	334	.2460
600 c/s	597	.4400
800 c/s	1030	.7600
1.0 kc/s	1357	1.0000
1.2 kc/s	1112	.8210
1.5 kc/s	705	.5200
2.0 kc/s	427	.3150
3.0 kc/s	255	.1880
4.0 kc/s	180	.1330
8.0 kc/s	87	.0642
10.0 kc/s	68	.0502
20.0 kc/s	31	.0227
40.0 kc/s	12	.0092

Table 10. Overall Voltage Gain for β = .00804

Frequency	$\lvert E_2/E_1 \rvert$	Normalized
20 c/s	7	.0050
60 c/s	19	.0146
100 c/s	33	.0242
200 c/s	68	.0502
300 c/s	107	.0794
400 c/s	152	.1125
800 c/s	623	.4620
1.0 kc/s	1356	1.0000
1.2 kc/s	718	.5310
1.5 kc/s	360	.2660
2.0 kc/s	205	.1520
4.0 kc/s	84	.0620
8.0 kc/s	39	.0290
10.0 kc/s	32	.0235
20.0 kc/s	16	.0118
40.0 kc/s	9	.0065

Table 11. Overall Voltage Gain for $\beta = .0269$

Frequency	$\lvert E_2/E_1 \rvert$	Normalized
20 c/s	4	.0029
60 c/s	8	.0059
100 c/s	13	.0094
200 c/s	26	.0191
300 c/s	40	.0294
400 c/s	58	.0432
800 c/s	256	.1900
900 c/s	510	.3775
1.0 kc/s	1355	1.0000
1.1 kc/s	544	.4030
1.2 kc/s	316	.2340
1.5 kc/s	138	.1020
2.0 kc/s	79	.0580
3.0 kc/s	43	.0318
4.0 kc/s	31	.0231
8.0 kc/s	15	.0113
10.0 kc/s	12	.0091
20.0 kc/s	6	.0047
40.0 kc/s	4	.0030

Table 12. Overall Voltage Gain for $\beta = .128$

Frequency	$\lvert E_2/E_1 \rvert$	Normalized
300 c/s	7	.0052
400 c/s	10	.0074
800 c/s	44	.0324
1.0 kc/s	1357	1.0000
1.2 kc/s	55	.0406
1.5 kc/s	24	.0177
2.0 kc/s	13	.0096

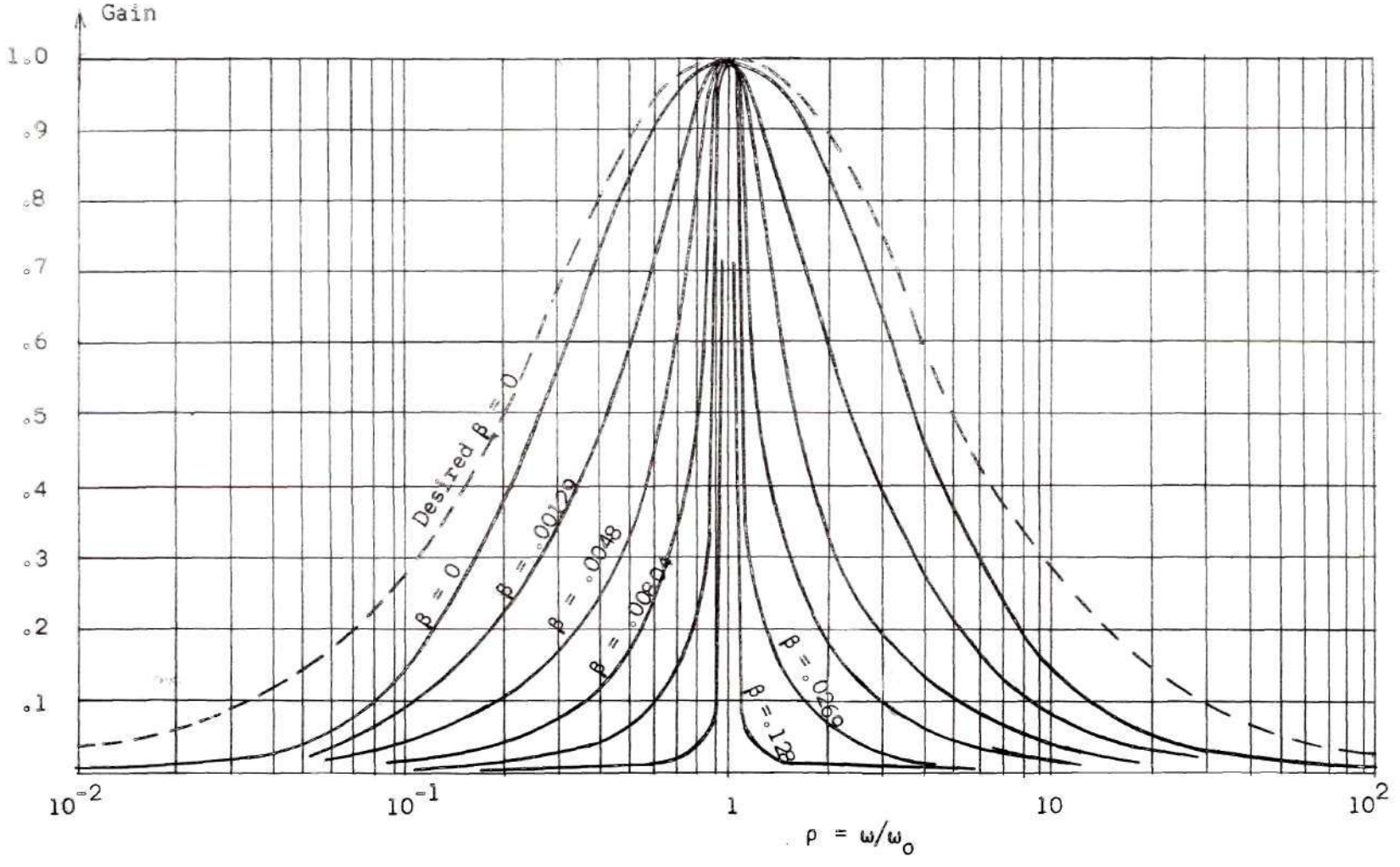


Figure 47. Normalized Frequency Response for Overall Circuit.

Table 13 contains the values for $|E_2/E_1|$ when $\beta = 1$ in the frequency range from 900 c/s to 1100 c/s. This data is normalized to unity and plotted in Figure 48. Now, recall Equation (8) in Chapter II which is restated as

$$\frac{E_2}{E_1} = \frac{K_e \omega_o}{Q_o(1 + \beta K_o)} \cdot \frac{S}{\left(S^2 + S\frac{\omega_o}{Q_o(1 + \beta K_o)} + \omega_o^2\right)}$$

When $\beta = 1$ the term $Q_o(1 + \beta K_o)$ corresponds to Q_{max} allowing the above equation to be rewritten as

$$\frac{1}{K_e} \cdot \frac{E_2}{E_1} = \frac{j\omega\omega_o}{Q_{max}(\omega_o^2 - \omega^2) + j\omega\omega_o}$$

where it has been normalized to unity at $f_o = 1$ kc/s. Dividing numerator and denominator by ω_o^2 and letting $\rho = \omega/\omega_o$ it can be written that

$$\left|\frac{1}{K_e} \cdot \frac{E_2}{E_1}\right| = \frac{\rho}{\sqrt{(1 - \rho^2)^2 Q_{max}^2 + \rho^2}} \qquad (43)$$

Equation (43) is plotted in Figure 48 for a Q_{max} of 400, 500 and 600 in order to compare the experimental response for $\beta = 1$ with these three values for Q_{max}. In the frequency region where $\rho < 1$ the experimental curve of Figure 48 is seen to resemble a curve for $Q_{max} \cong 570$. However, in the region for $\rho > 1$ the experimental curve has a mean value following a $Q_{max} \cong 450$ curve. It would be safe to simply rely on

Table 13. Overall Voltage Gain for $\beta = 1$

Frequency	$\lvert E_2/E_1 \rvert$	Normalized
900 c/s	12.0	.0088
910 c/s	13.2	.0097
920 c/s	14.9	.0110
930 c/s	17.0	.0125
940 c/s	19.9	.0146
950 c/s	23.8	.0175
960 c/s	29.7	.0218
970 c/s	38.7	.0285
980 c/s	58.2	.0427
990 c/s	107.0	.0786
995 c/s	151.0	.1110
1000 c/s	1360.0	1.0000
1005 c/s	444.4	.3260
1010 c/s	174.0	.1280
1020 c/s	75.2	.0553
1030 c/s	46.5	.0342
1040 c/s	34.6	.0254
1050 c/s	28.6	.0210
1060 c/s	22.5	.0165
1070 c/s	19.8	.0145
1080 c/s	17.0	.0125
1090 c/s	15.2	.0112
1100 c/s	13.2	.0097

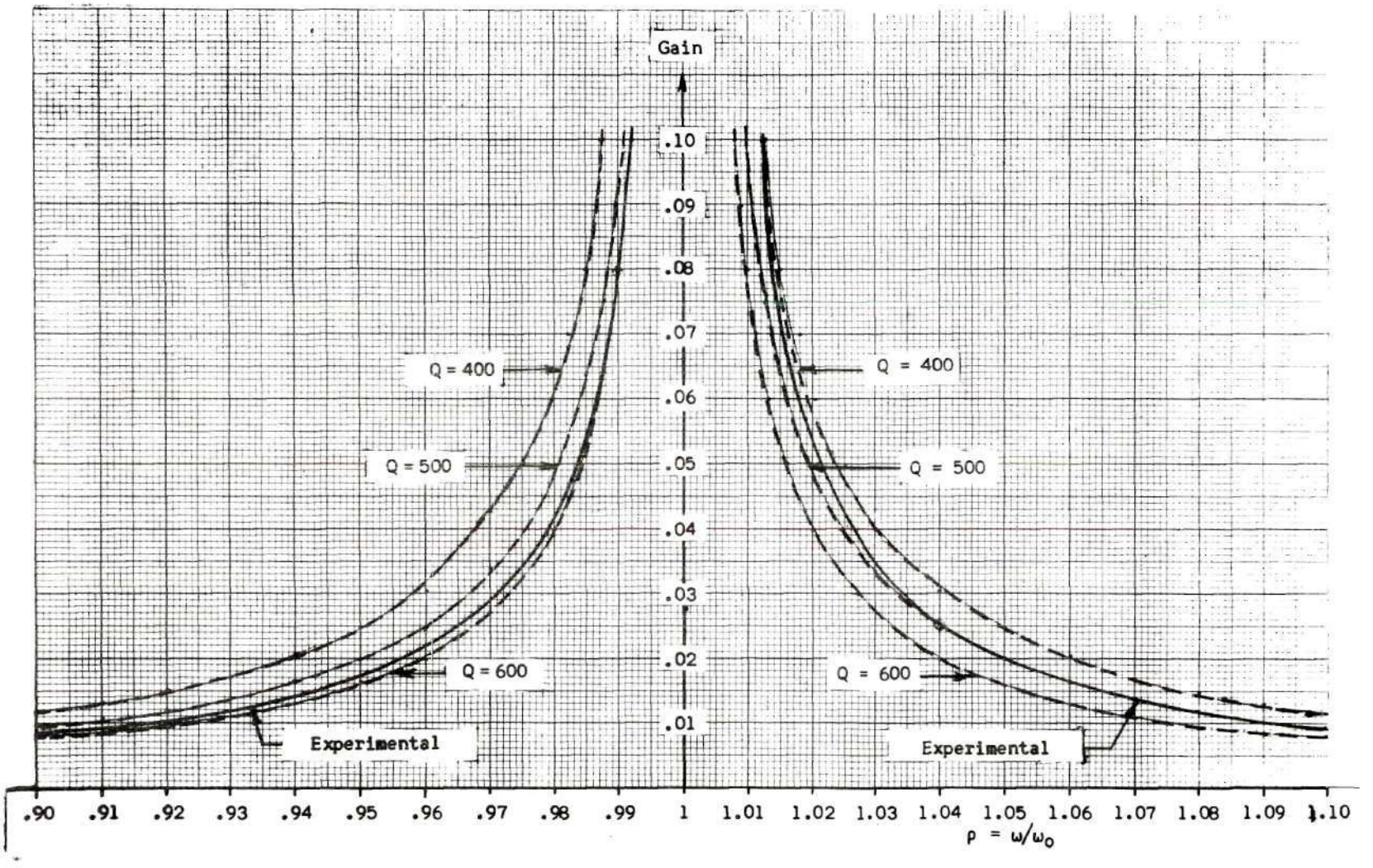


Figure 48. Normalized Frequency Response for $\beta = 1$.

$$Q_{max} \cong \frac{\left|\frac{E_2}{E_1}\right|_{f_o}}{2.71} \cong 503$$

as was to be expected. To determine the actual half-power bandwidth for this experimental curve and use

$$Q_{max} = \frac{f_o}{\text{Bandwidth}}$$

would be difficult since the bandwidth will be on the order of

$$B.W. \sim \frac{f_o}{Q_{max}} = \frac{1000}{500} = 2 \text{ c/s}$$

The available measuring instruments could not approach making such a measurement with any accuracy.

For values of β from zero to unity the voltage gain, E_2/E_1, at 1 kc/s appeared to remain fairly constant. The slight .37% decrease in this gain, as evidenced in Tables 7 through 12, could have been avoided by periodically checking the tuning of the parallel-T. (i.e. simply adjust a variable tuning element in the parallel-T to make the gain remain constant as β is increased.) However, for most purposes the slight decrease in gain experienced here would be insignificant. The maximum gain always occurred at f_o = 1 kc/s for β varied from zero to unity. This is, of course, because the amplitude response for the amplifier section is symmetrical about f_o = 1 kc/s as can be seen in Figure 42.

The 4$\mu\mu$f and 20 $\mu\mu$f capacitors shown in Figure 49 are to correct the closed loop phase shift and prevent oscillation. In Figure 49b

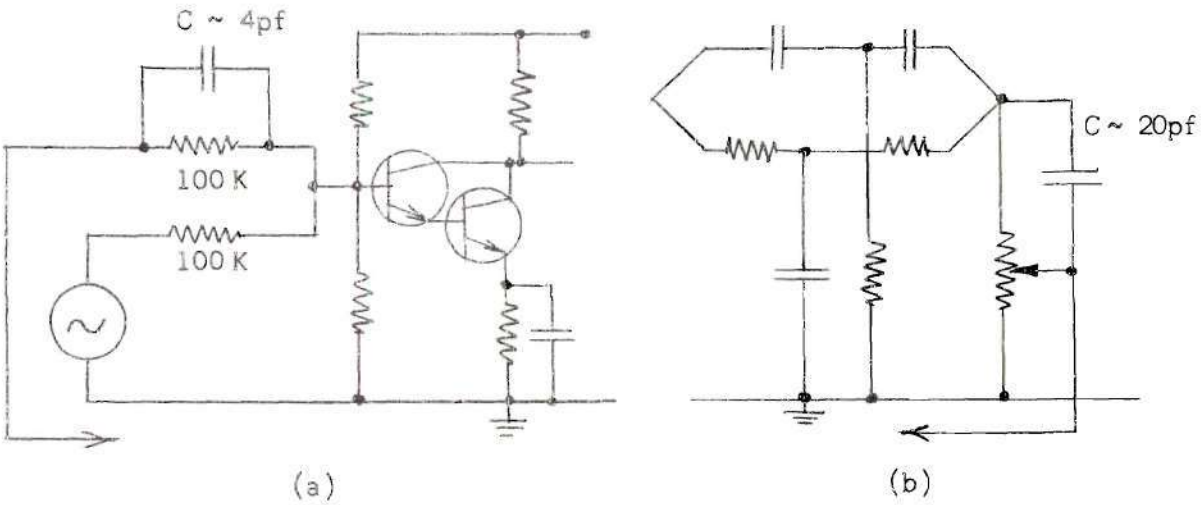


Figure 49. Partial Circuits Showing Capacitors for Phase Correction

the capacitor C ~ 20 μμf has about the same value as the parasitic capacitance of the shielded cable used for the feedback lead. Experience has shown that the 4 μμf capacitor in the experimental circuit has the greater effect on overall stability with the 20 μμf capacitor having only a slight effect. For instance, if the 20 μμf capacitor were removed the output voltage would become only slightly unstable for $\beta = 1$. It would not actually break into oscillation but would fluctuate in magnitude somewhat. However, if the 4 μμf capacitor were removed oscillations would begin when β reached .147. The oscillation would be at a frequency near or equal to 1 kc/s. Recall that the overall circuit Q is

$$Q = Q_o(1 + \beta K_o) = .354(1 + \beta K_o)$$

and

$$Q_{max} = .354(1 + K_o)$$

For the present circuit $Q_{max} \sim 500$ and

$$K_o \sim \frac{500}{.354} - 1 = 1,412$$

so

$$\text{Overall } Q = .354\,[1 + \beta(1,412)]$$

Now for $\beta = .147$

$$Q = .354\,[1 + (.147)(1,412)] = 73.5$$

Therefore, the presence of the $4\mu\mu f$ capacitor allows the overall Q-factor to increase from 73.5 to 500 without oscillations.

As previously discussed, the minimum possible input voltage will be determined by the noise level in the circuit while the maximum possible input voltage will be determined by clipping in the last transistor stage. Maximum and minimum input voltages were measured for $\beta = 0$, and $\beta = 1$. These measurements appear in Table 14.

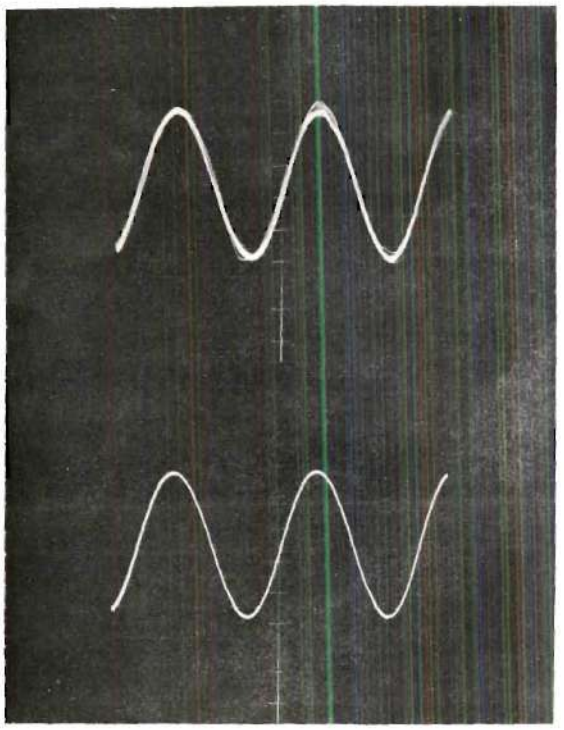
Table 14. Input Voltage Extremes

	$\beta = 0$	$\beta = 1$
Maximum Input at $f_o = 1$ kc/s in volts rms	1.48×10^{-3}	2.59×10^{-3}
Minimum Input at $f_o = 1$ kc/s in volts rms	$.148 \times 10^{-3}$	~ 0

Note, from Table 14, that with feedback a larger range for input voltages is possible. Not only does the negative feedback correct distortion up to a certain point, but it also eliminates all visible traces of noise. Figure 50 is a photograph of the output voltage showing the effect of feedback on the circuit noise. The waveforms in Figure 50 are for an input voltage of $.1 \times 10^{-3}$ volt rms. Figure 50a is for $\beta = 0$ and Figure 50b is for $\beta = 1$. However, the noise will clear up for β only slightly greater than zero. Figure 51 is a photograph illustrating the effect of feedback on distortion in the output. The waveforms here are for an input voltage of 2.37×10^{-3} volt rms. Figure 51a is for $\beta = 0$ and Figure 51b is for β any value slightly greater than zero to unity.

It will be instructive to consider the effect on the overall voltage gain, E_2/E_1, as the d.c. supply voltage is varied. Recall from Figure 38 that a 30 volt source and a 60 volt source are used in the circuit. The effects of varying these voltages separately and varying them simultaneously will be considered. The results are presented in Table 15. The results here are almost the same for any value of β.

Also, it will be instructive to consider the effects of increasing the temperature in the vicinity of the entire circuit. All measurements made to this point were made at $T \sim 77^{\circ}$ F. The temperature was raised to $T \sim 130^{\circ}$ F and the voltage gain at 1 kc/s increased from 1,355 to 1,540 or about a 14% increase in gain. This was for $\beta = 0$. However, as β was increased to unity the output vanished indicating that the parallel-T was out of tune. The output voltage was restored by adjusting the variable elements in the parallel-T until the output had reached the desired level. Upon cooling, the bridge again had to be tuned to keep a constant



a.

b.

Figure 50. Effect of Feedback on Noise.

a.

b.

Figure 51. Effect of Feedback on Distortion

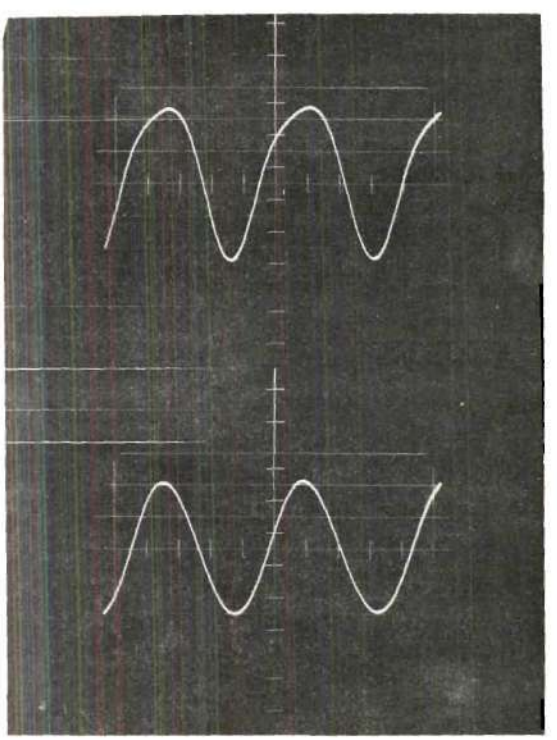


Table 15. Effect of Changing D.C. Supply Voltages

D.C. Supplies	$\lvert E_2/E_1 \rvert$	% Change in $\lvert E_2/E_1 \rvert$
30 v. 60 v.	1355	
30 v. up 20% 60 v. same	1780	31% increase
30 v. down 20% 60 v. same	893	34% decrease
30 v. same 60 v. up 20%	1565	16% increase
30 v. same 60 v. down 20%	1065	21% decrease
30 v. up 20% 60 v. up 20%	2090	54% increase
30 v. down 20% 60 v. down 20%	711	48% decrease
30 v. up 10% 60 v. same	1565	16% increase
30 v. down 10% 60 v. same	1168	14% decrease
30 v. same 60 v. up 10%	1453	7% increase
30 v. same 60 v. down 10%	1219	10% decrease

gain at center frequency as β is varied.

To illustrate the high selectivity of the experimental circuit as β is increased, a 1 kc/s square wave input was used. From Fourier theory a square wave with a peak-to-peak voltage of V volts is given by

$$v(\omega t) = \frac{2V}{\pi} (\cos \omega t - \frac{1}{3} \cos 3 \omega t + \frac{1}{5} \cos 5 \omega t$$

$$- \frac{1}{7} \cos 7 \omega t + \ldots\ldots\ldots).$$

For a square wave at 1 kc/s the 1 kc/s Fourier component is

$$\frac{2V}{\pi} \cos \omega t$$

Figure 52a is a photograph of the square wave input having a peak-to-peak voltage of 2×10^{-3} volt. Figure 52b is the output for $\beta = 0$ where harmonics are present. However, for β made slightly greater than zero to unity the output appears as in Figure 52c. This is a 1 kc/s sine wave with a peak-to-peak value of 3.45 volts. This is in good agreement with Fourier theory as follows:

$$\text{Input component at 1 kc/s} = \frac{2V}{\pi} \cos \omega t = \frac{(2)(2 \times 10^{-3})}{\pi} \cos \omega t$$

$$\text{Voltage Gain at 1 kc/s} = 1,355$$

$$\text{Expected output} = \frac{(1.355 \times 10^{3})(4 \times 10^{-3})}{\pi} \cos \omega t$$

$$= 1.728 \cos \omega t$$

which has a peak-to-peak value of 3.46 volts.

Therefore, the harmonics have been eliminated and only the 1 kc/s component is passed and amplified.

a.

b.

c.

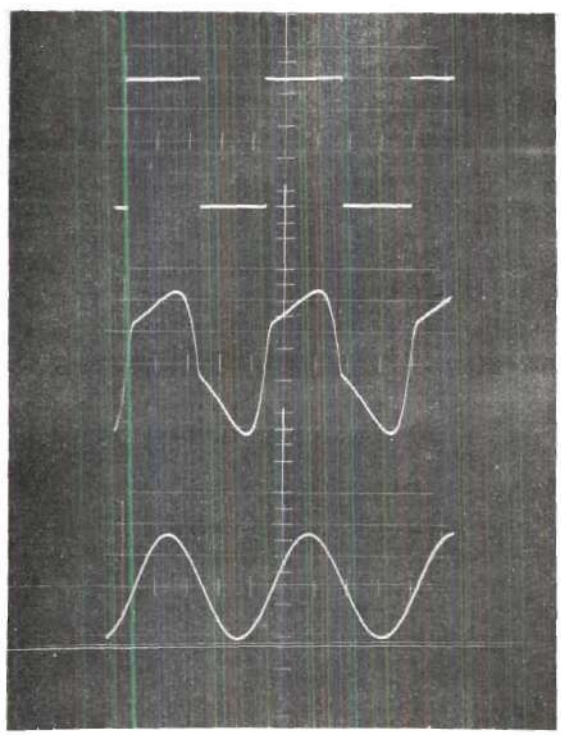


Figure 52. Output Voltage for Zero Feedback and Maximum Feedback with Square Wave Input.

CHAPTER V

CONCLUSIONS AND RECOMMENDATIONS

Physical Limitations for Proposed Problem

The method used for solving the proposed problem has certain physical limitations that affect the overall circuit operation. It will now be beneficial to recapitulate the major limitations encountered in circuit design and operation of the proposed circuit.

The possibility of oscillation is present in any circuit involving feedback unless care is exercised in design. The threat of oscillation forms an upper limit on the Q_{max} attained in the present circuit. This is because the greater the Q_{max} is to be the greater the voltage gain must be as can be seen from Equation (40). Therefore, it will be more difficult to make the closed loop voltage gain reach 0 db before the phase shift around the loop reaches 180°. Experimentation was plagued by oscillations at $f \sim 1$ kc/s and $f \gg 1$ kc/s as β was increased from zero. However, the high frequency oscillation could usually be predicted by sketching the frequency response for both amplitude and phase shift and assuming oscillations would occur near the frequency where the phase shift reached 180° and the closed loop gain was greater than 0 db. Without the phase correction techniques employed for the series feedback resistor and the output resistor on the parallel-T the stable $Q_{max} \sim 500$ could not have been achieved. Actually, $Q_{max} \sim 500$ appeared to be the highest stable Q attainable with the design used (i.e. with the values of n, K and

$1/G_o$ chosen and with two narrowband and one wideband amplifier stage.)

Noise was apparent in the final output for $\beta \cong 0$. An attempt was made to achieve a high signal-to-noise ratio at the output to the first stage by having a fairly high voltage gain in this stage, but this did not eliminate all traces of noise in the output. The large biasing resistors in the first stage no doubt contribute to the noise problem as predicted by the following Nyquist relation for thermal noise:

$$\text{R.M.S. Noise} = E_n = \sqrt{4kRT(BW)}$$

where k = Boltzmann's constant

$= 1.38 \times 10^{-23}$ watt-sec/degree Kelvin

R = resistance of conductor

T = temperature of conductor in degrees Kelvin

B.W. = bandwidth of the measuring system in cycles per second.

Also, thermal noise, shot noise and $1/f$ noise associated with the transistors in the input stage will contribute to the overall noise problem. However, as β is made greater than zero the negative feedback eliminates the noise at the output of the load circuit. Fortunately, the noise disappears rapidly as β is increased. If circuit operation is desired for $\beta \cong 0$, the noise level will set the lower limit on the input signal magnitude while the size of the dynamic path on the last amplifying stage will decide the upper limit on the input signal.

It is difficult to design the amplifier section with a bandwidth several times that of f_o/Q_o while meeting other circuit criteria. If the amplifier bandwidth is too narrow the overall circuit, for $\beta = 0$, will have a bandwidth less than the desired f_o/Q_o. For some applications

this fact may not matter, but for others it may prove a severe handicap. The experimental circuit's amplifier was made too narrow in an effort to achieve stable operation.

The operation of the parallel-T is easily affected resulting in changes in the overall circuit operation. It should also be noted that the null at the resonant frequency f_o is not perfect and the attenuation here is finite. If the parallel-T is to be used in a wide temperature range, very stable components would be necessary for all of its circuit elements. Also, the solder connections in the parallel-T network should be made with care to insure good results. Good solder joints are, of course, important throughout, but experience has shown that one cold joint in the parallel-T can cause particular frustration.

The fact that high-gain voltage amplifiers are needed for circuit operation requires a certain amount of shielding. In particular, all leads from the external equipment were shielded to prevent unwanted effects. For instance, 60 c/s from the overhead lighting was continuously apparent in the final output. Also, the parasitic capacitive coupling between stages had a drastic effect on the stability of transistor Q-points. While the construction of aluminum boxes for each stage helped the situation it did not eliminate it. It was generally advisable to use short leads in the circuit where possible and even use shielded cable for some internal wiring such as the feedback wire to the input stage. A good circuit ground had a profound effect on the overall circuit operation. For the experimental circuit a bench ground was used to prevent the output signal from jumping about. The bench ground was only connected to one external instrument, as shown in Figure 53b, to prevent currents from flowing in a

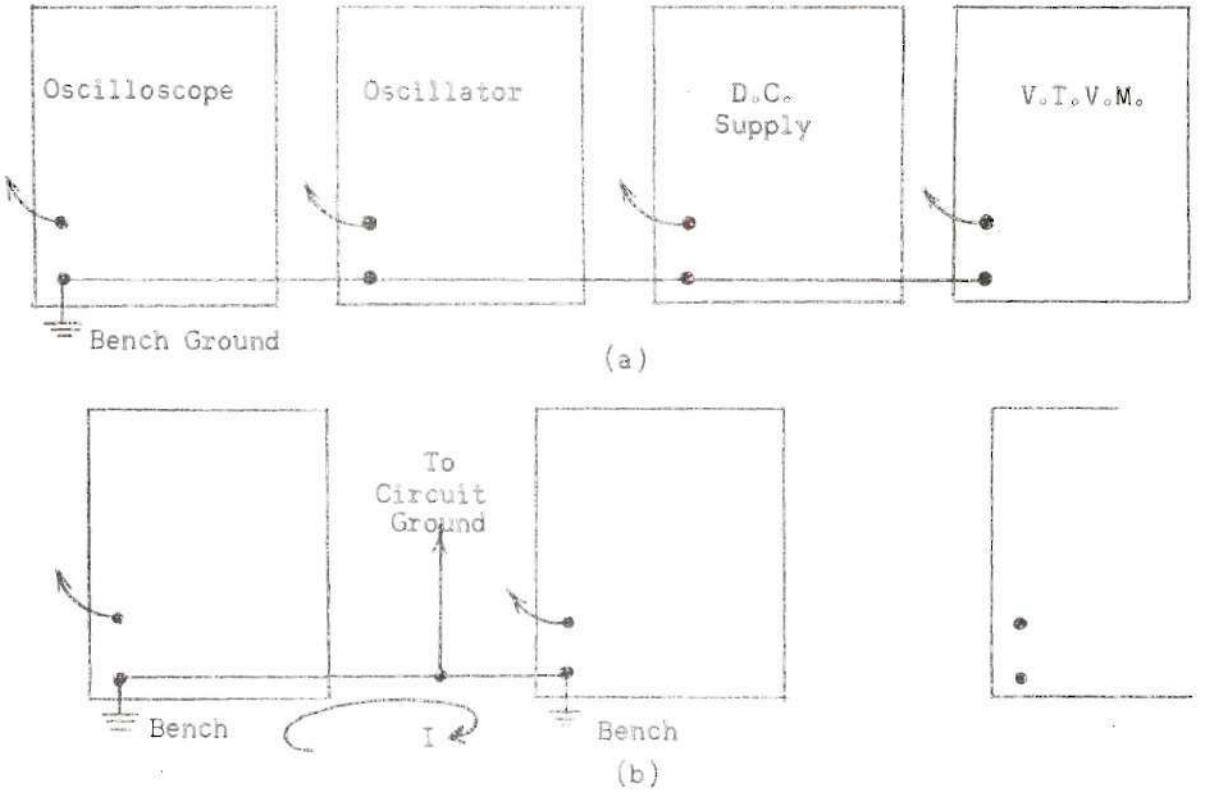


Figure 53. Instrument Arrangement to Prevent Ground Loop Currents.

ground loop as shown in Figure 53b. In Figure 53b both the oscilloscope and oscillator have their chassis grounds connected to the bench ground. Here, the ground loop current can flow contributing to the overall noise problem and causing the output to jump about.

Other Possibilities for Solution to Proposed Problem

While the solution to the proposed problem as presented may be satisfactory for some applications it will be worthwhile to consider other possibilities for solution to improve operation and allow achievement of a higher Q_{max}.

The use of two special wideband amplifier stages and one narrowband

stage possibly could be made to produce stable operation with the overall amplifier bandwidth much greater than f_o/Q_o. Several texts on transistor circuit design contain complete schematics for wideband amplifiers with a bandwidth of about 20 mc/s. With slight alterations most of these amplifiers could be applied to the problem at hand. Then, if necessary, special phase correction techniques could be used to make the closed loop voltage gain reach 0 db before the phase shift reached 180°.

It will be worthwhile to consider application of the field-effect transistor to the proposed problem. The field-effect transistor has the attractive feature that the input resistance can be made in the range 1 to 100 megohms. Also, this transistor has a fairly low noise figure and could be used to produce a fairly high voltage gain. In addition, a typical unit would have a cutoff frequency of several megacycles per second. These features could prove extremely valuable for possible use in the input stage whether it was a summing stage or a differential stage.

The selection of n, K and $1/G_o$ could be changed to allow the circuit to produce a higher Q_{max} for the same voltage gain. For instance, the following choices in these parameters could make significant improvements:

$$n = 1.62$$

$$K = .1$$

$$1/G_o = 15\ K\Omega$$

where the parallel-T works into 150 KΩ.

Although a summing amplifier was chosen for the experimental circuit it is, of course, also possible to use a difference amplifier for the

input stage. This would have the advantage of requiring only two amplifier stages thereby decreasing the stability problem. The difference amplifier could be designed to produce sufficient gain so that, upon coupling to the second stage, Q's greater than 500 could be achieved. Also, the bandwidth of the amplifier section could probably be made wide enough for correct operation of the overall circuit without oscillations occurring since the phase shift for the amplifier would approach 180° at both high and low frequencies.

Changing the entire problem from one of voltage feedback to one of current feedback could produce the same overall results while eliminating many disadvantages of voltage feedback. The transistor is basically a current amplifier and current feedback would utilize this property instead of attempting to create a high gain voltage amplifier.

A P P E N D I X

APPENDIX

Parallel-T Tuning Procedure

It will be necessary to leave certain elements in the parallel-T network variable in order to tune for the best null at f_o = 1 kc/s. However, even the procedure to be presented here will not achieve a perfect notch at f_o.

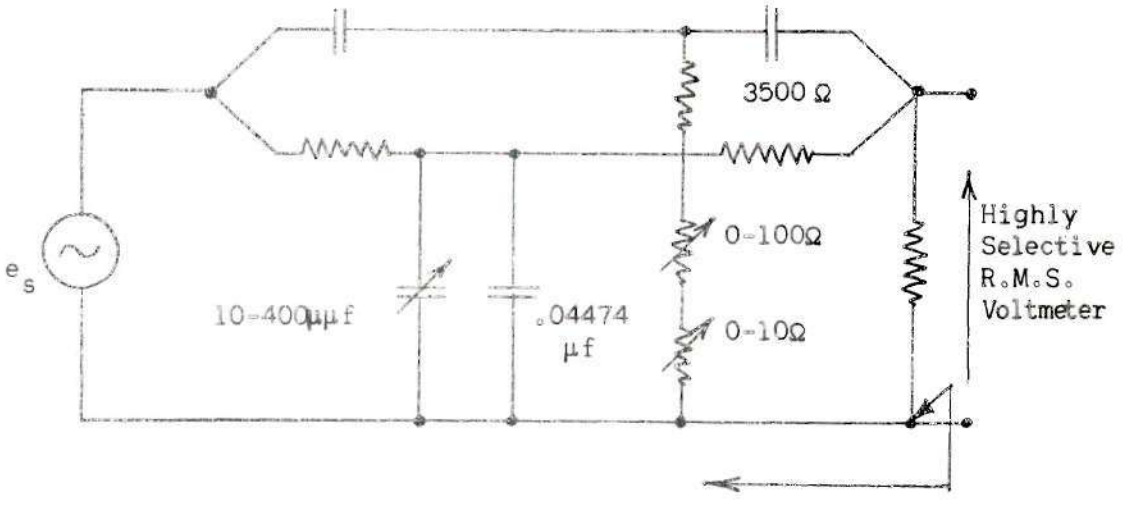


Figure 54. Circuit for Tuning Parallel-T

Figure 54 shows the capacitor and resistor to be left variable in the parallel-T. Note that the input resistor, $1/G_o$, is not shown since it and $1/G_1$ will comprise the load resistance on the last transistor stage and it is not needed here for tuning. The input signal should be applied as shown in Figure 21 and should be set at f_o = 1 kc/s. The output will be observed with a highly selective r.m.s. voltmeter such as the General Radio Wave Analyzer. A wideband voltmeter will not suffice

because it will pass, and measure, the harmonic content of the signal source. The harmonics are, of course, passed through the parallel-T network without much attenuation. Thus, once the signal at $f = f_o$ is nulled to a value less than the harmonic content the meter reading will be meaningless as regards tuning.

A procedure for initially tuning the parallel-T is outlined as follows:

(a) Set signal source to $f = 1$ kc/s.

(b) With the r.m.s. voltmeter on the parallel-T output adjust the voltmeter's frequency control until its meter reads maximum. This will center its passband at 1 kc/s.

(c) Adjust the variable 100 Ω resistor for an output minimum.

(d) Adjust the 400 pf capacitor for an output minimum.

(e) Again adjust the frequency control on the voltmeter for a maximum meter reading.

(f) Adjust the variable 10 Ω resistor for an output minimum. etc.

Final tuning for the parallel-T is best performed under actual operating conditions. This final tuning utilizes the fact that the output voltage for the load circuit should remain constant for $f = 1$ kc/s as β is varied from zero to unity. With reference to Figure 55 the output voltage E_2 will be held constant by adjusting R and C as the feedback arm is varied from ground upward. β should be raised from zero in small discrete steps and the frequency of the input source should be adjusted at each step to assure that it is on resonance. In particular, for β near unity and a large overall Q-factor the frequency adjustment on E_1 is important because the overall bandwidth is so small.

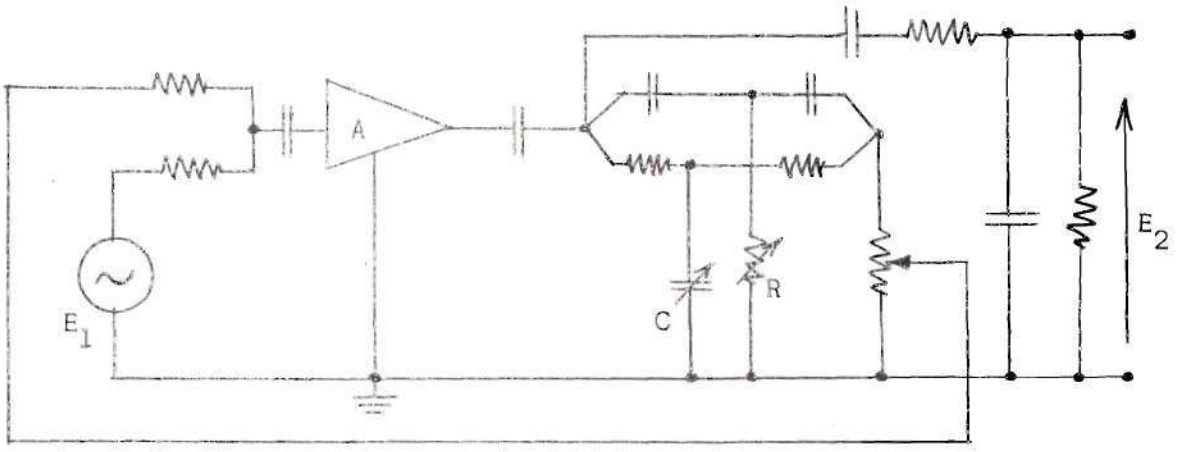


Figure 55. Entire Circuit Used for Final Tuning of Parallel-T.

Since tuning is possible in the parallel-T it should be possible to use normal tolerance components in it. However, the circuit elements used in the experimental circuit were all measured on an impedance bridge to minimize the tuning necessary.

Plotting Dynamic Operating Path

A procedure for plotting the dynamic operating path (i.e. i_C vs. v_{CE}) for the last transistor stage will now be given. Figure 56 shows a portion of the circuit useful in this analysis.

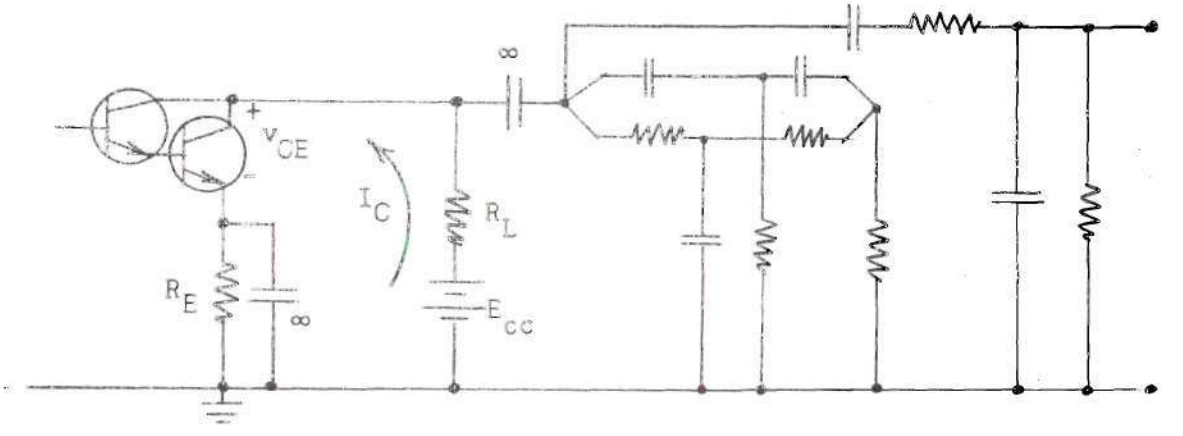


Figure 56. Circuit for Analysis of D.O.P.

Instantaneous i_C = d.c. current + a.c. current

$$= I_C + i_c$$

$$i_C = I_C + A \sin \omega t \tag{44}$$

Now assume $I_C \sim I_E$ and $i_c \sim i_e$ and write

$$v_{CE} \tilde{=} E_{CC} - I_C R_L - i_c |Z_{11T} \| Z_{11L}| \angle\theta - I_C R_E$$

$$v_{CE} \tilde{=} E_{CC} - I_C(R_L + R_E) - i_c |Z_{11T} \| Z_{11L}| \angle\theta$$

$$v_{CE} \tilde{=} E_{CC} - I_C(R_L + R_E) - A|Z_{11T} \| Z_{11L}| \sin(\omega t - \theta) \tag{45}$$

Now plot Equation (44) vs. Equation (45) as ωt varies from 0 to 2π.

In Equation (44) and Equation (45)

$$A = \frac{\text{peak-to-peak current on D.O.P.}}{2}$$

$|Z_{11T} \| Z_{11L}|$ can be determined for a particular frequency from Figure 15 in Chapter II. Also, θ associated with $|Z_{11T} \| Z_{11L}|$ is

$$\theta = \text{Tan}^{-1}\left(\frac{6.83\rho}{3.83 - \rho^2}\right) - \text{Tan}^{-1}\left(\frac{2.83\rho}{1 - \rho^2}\right)$$

for $n = 1$ as can be verified from the equations for $Z_{11T} \| Z_{11L}$ in Chapter II.

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